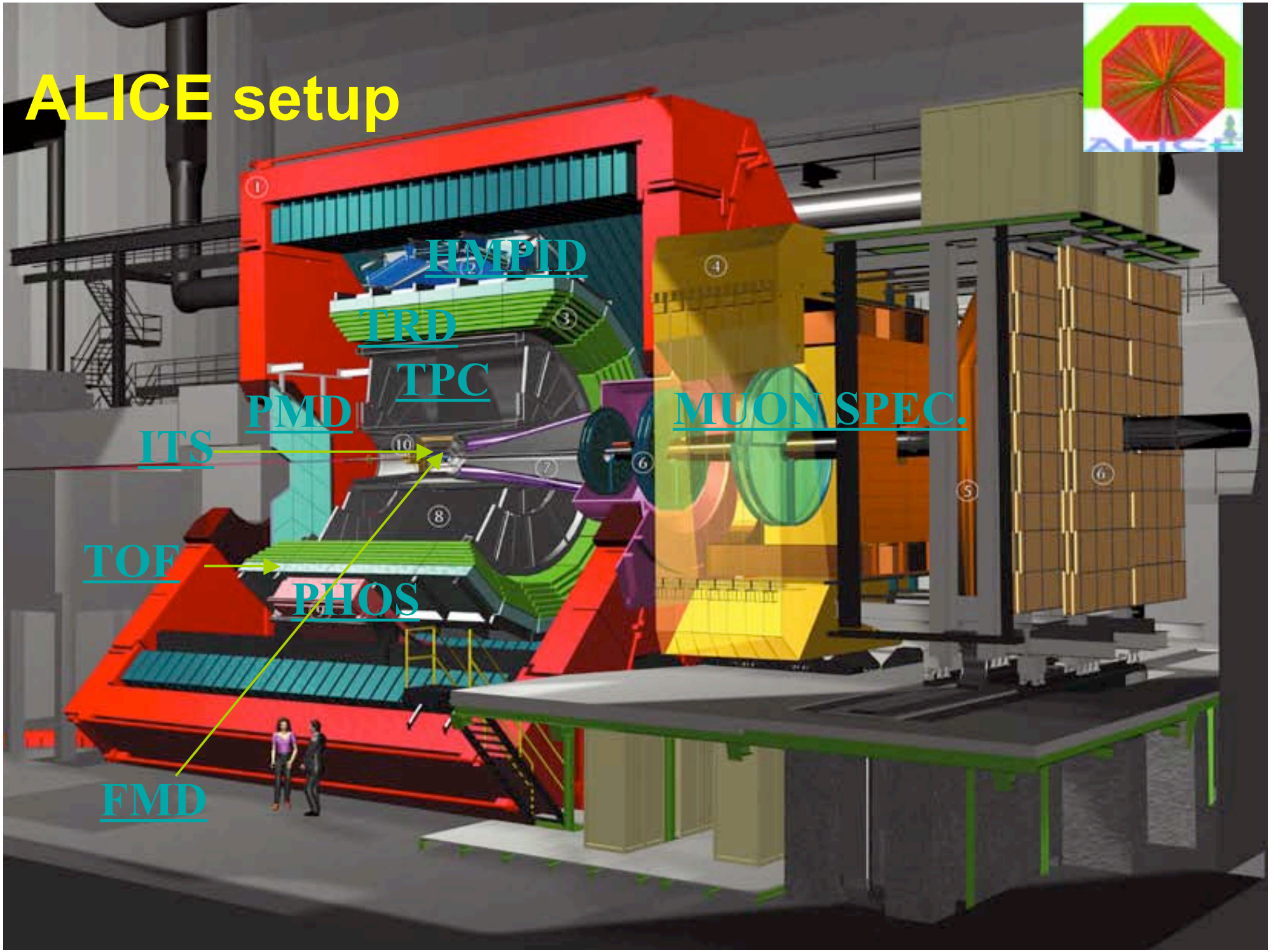

ALICE setup
HMPID
TRD
TPC
PMD
MUON SPEC.
ITS
TOF
PHOS
FMD

ALICE Physics goals

(has to cover in one experiment what at the SPS was covered by 6-7 experiments, and at RHIC by 4!!)

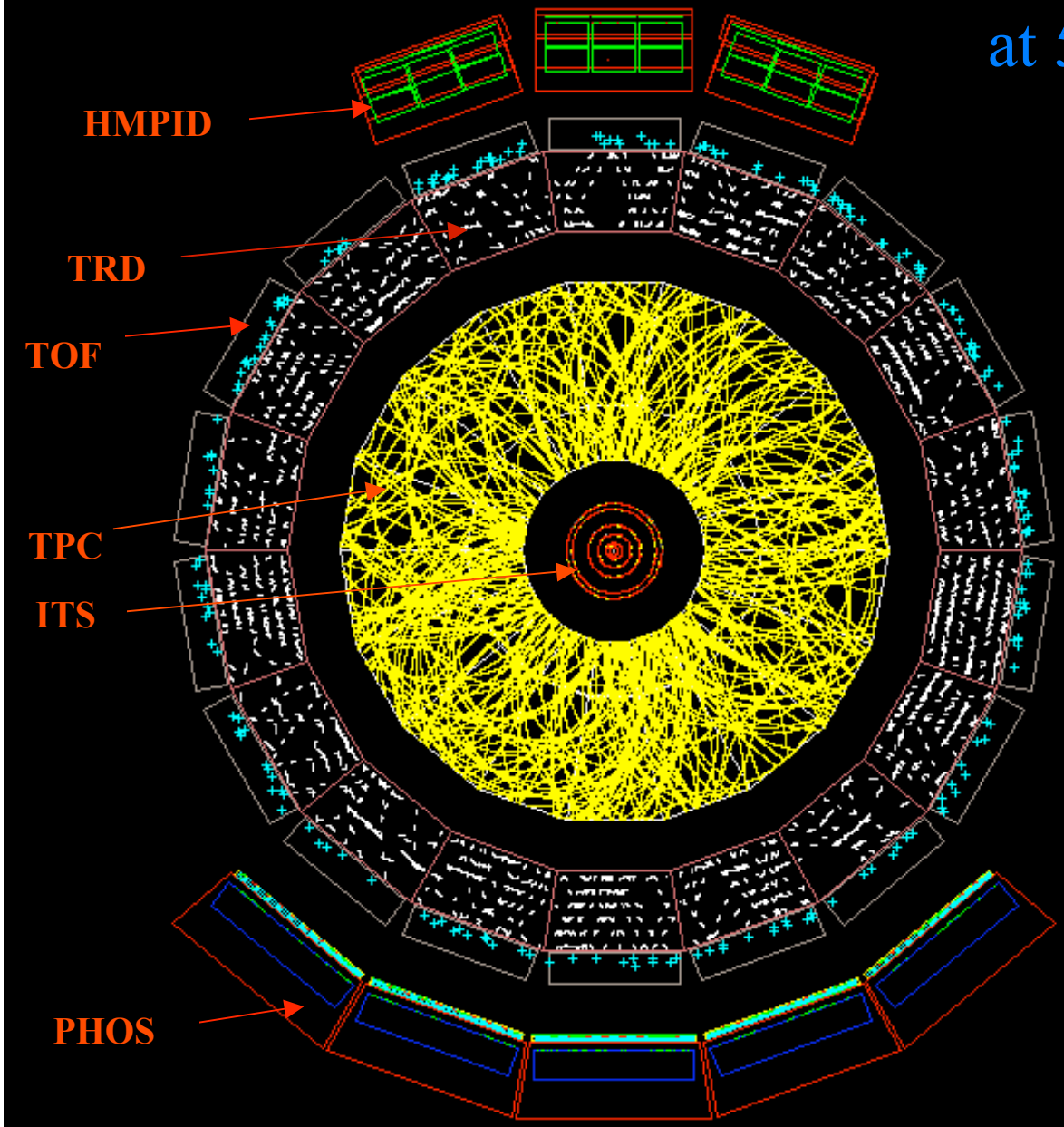
- **Global observables:**
  Multiplicities, η distributions
- **Degrees of freedom as a function of T** hadron ratios and spectra, dilepton continuum, direct photons
- **Early state manifestation of collective effects:**
  elliptic flow
- **Energy loss of partons in quark gluon plasma:**
  jet quenching, high pt spectra, open charm and open beauty

- **Deconfinement:**
  charmonium and bottonium spectroscopy
- **Chiral symmetry restoration:**
  neutral to charged ratios, res. decays
- **Fluctuation phenomena - critical behavior:**
  event-by-event particle comp. and spectra
- **Geometry of the emitting source:**
  HBT, impact parameter via zero-degree energy flow
- **pp collisions in a new energy domain**

- Large acceptance
- Good tracking capabilities
- Selective triggering
- Excellent granularity
- Wide momentum coverage
- P.I.D. of hadrons and leptons
- Good sec. vertex reconstr.
- Photon Detection

Use a variety of experimental techniques!

Studies of the ALICE Performance



5000 PbPb events
at 5.5 TeV/nucleon pair
were produced
for PPR

In this picture:
dNch/dη ~ 8000
(slice: 2° in θ)
84'210 primary particles

Data size

- **Hits ~1.4Gb**
- **Digits ~1.1Gb**

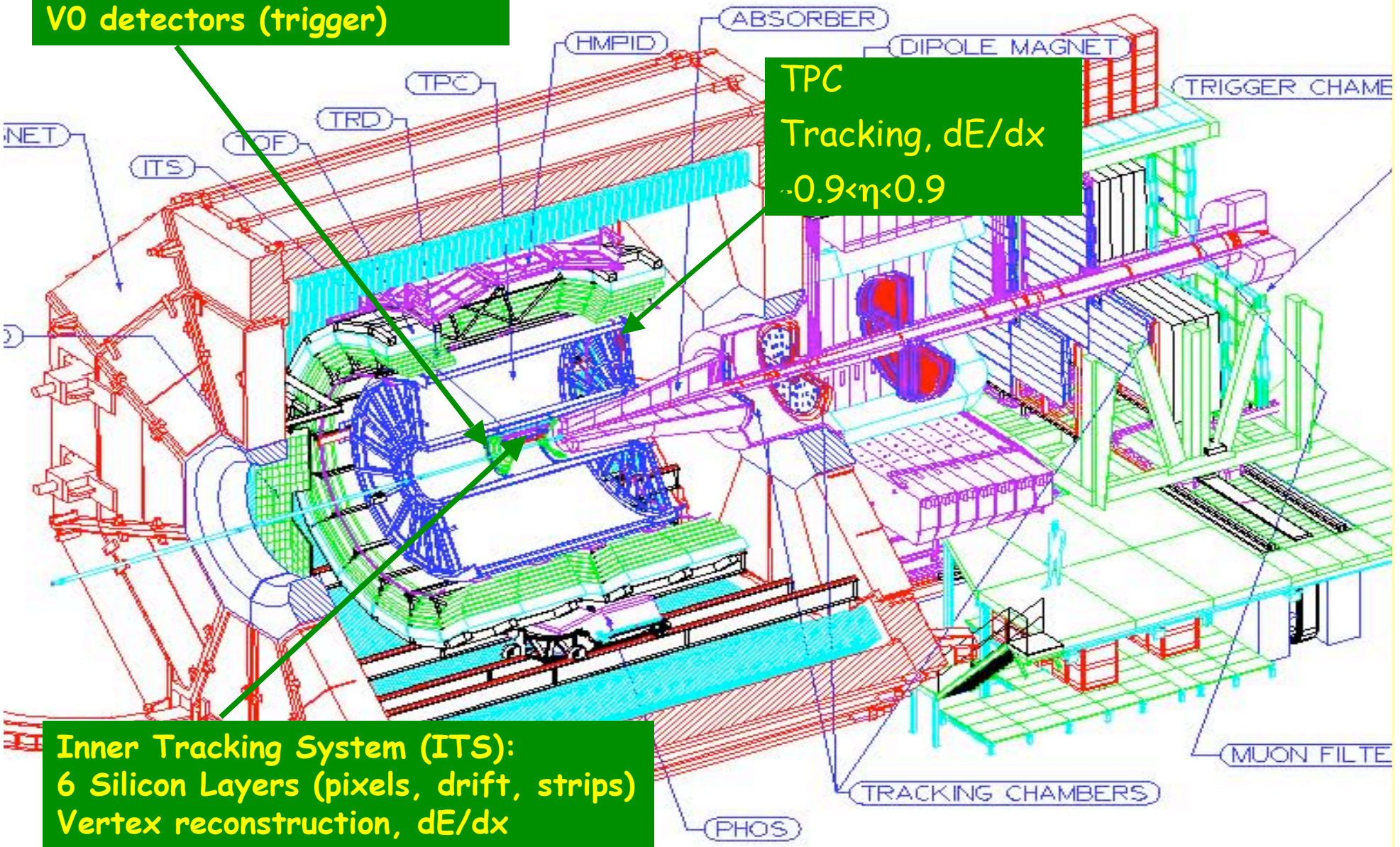
CPU time on 800MHz PIII

- **Hits ~24h**
- **Digits ~15h**

ALICE LAYOUT: TRACKING
(and event characterization)

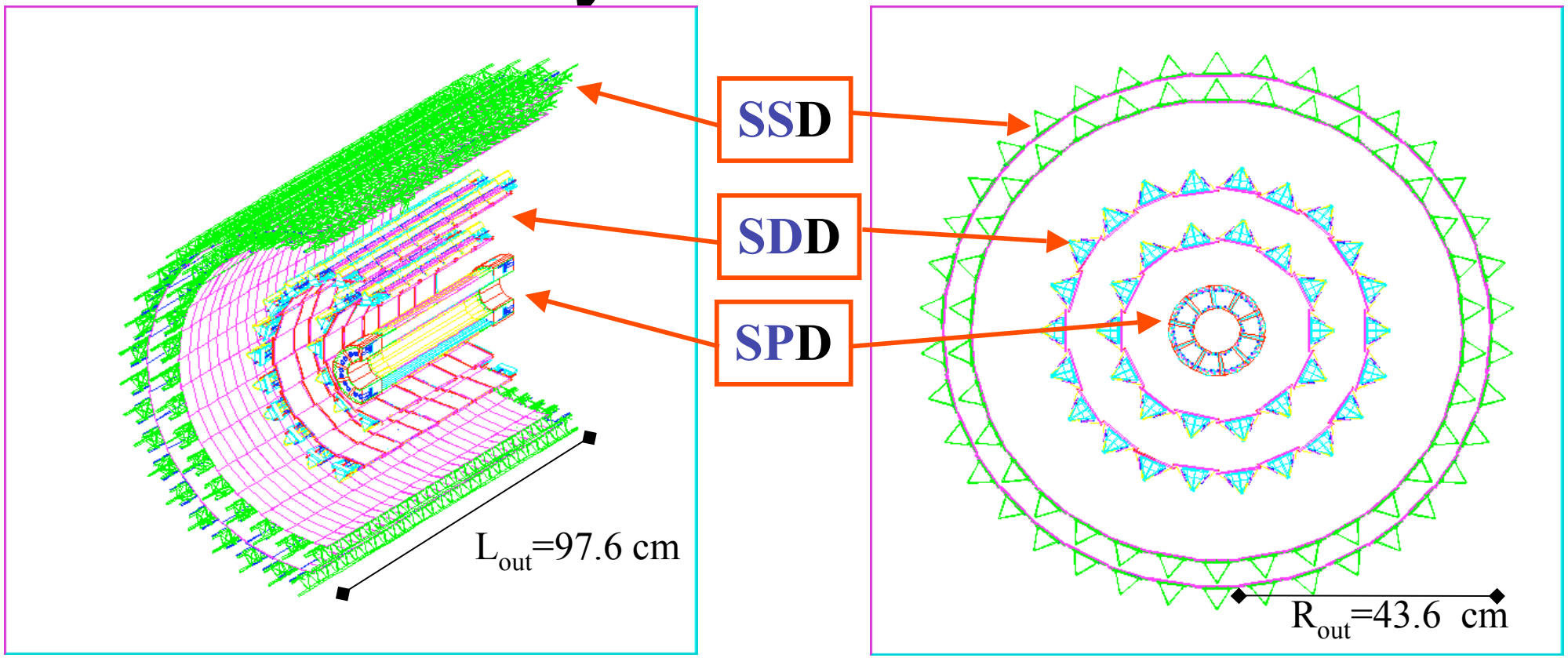
Forward Multiplicity Detectors
T0 detectors (event time)
V0 detectors (trigger)

TPC
Tracking, dE/dx
$-0.9<\eta<0.9$

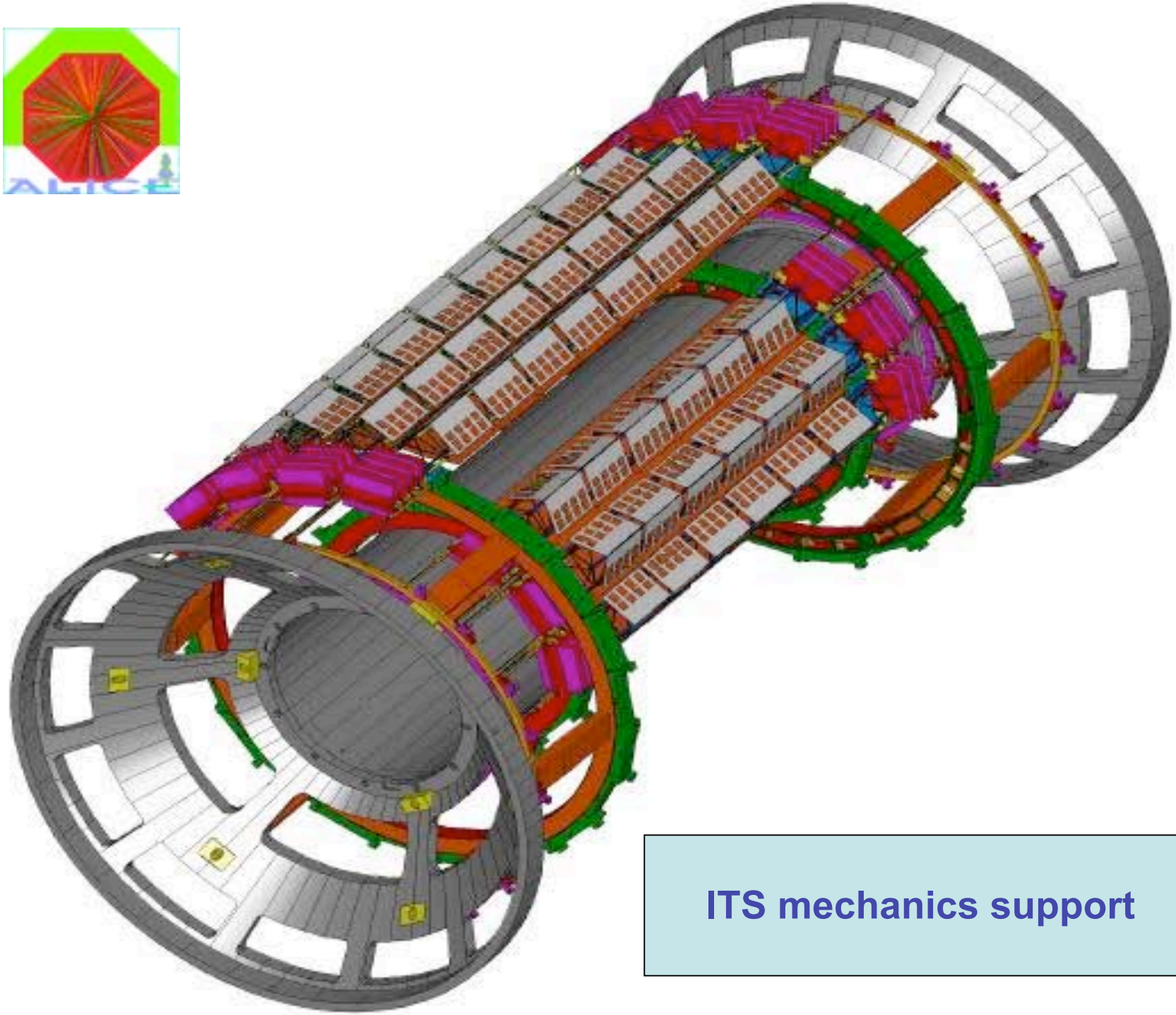


Inner Tracking System (ITS):
6 Silicon Layers (pixels, drift, strips)
Vertex reconstruction, dE/dx
$-0.9<\eta<0.9$

The ALICE Inner Tracking System - ITS



- **6** Layers, three technologies (keep occupancy ~constant **~2%** for max mult)
  - **1-2 S**ilicon **P**ixel (0.2 m^2, 9.8 Mchannels)
  - **3-4 S**ilicon **D**rift (1.3 m^2, 133 kchannels)
  - **5-6** Double-sided **S**ilicon **S**trip (4.9 m^2, 2.6 Mchannels)

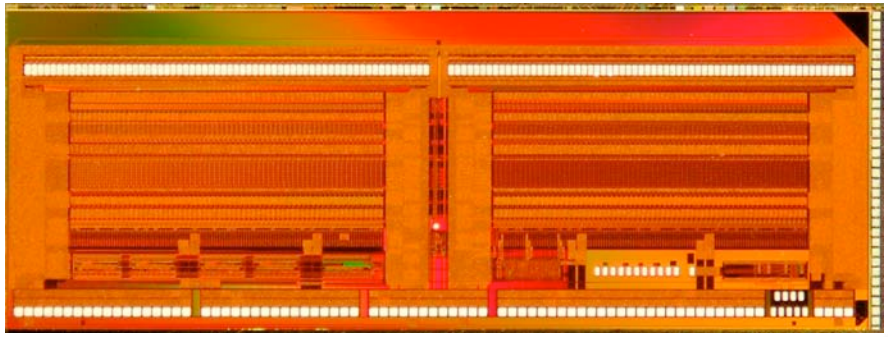


ITS mechanics support

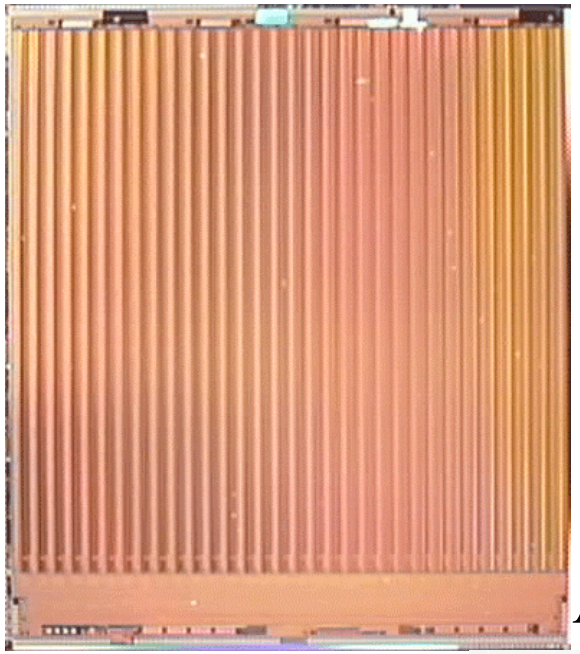
ITS: Many electronics developments

(all full-custom designs in rad. tol., 0.25 μm process)

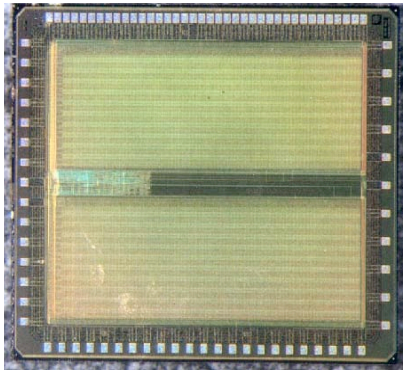
ALICE PIXEL CHIP
50 μm x 425 μm pixels
8192 cells
Area: 12.8 x 13.6 mm^2
13 million transistors
~100 μW/channel

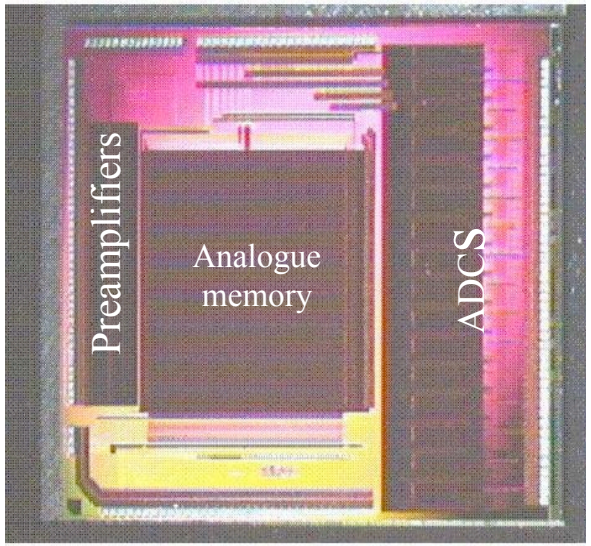


ALICE SSD FEE
HAL25 chip:
128 channels
Preamp+s/h+
serial out



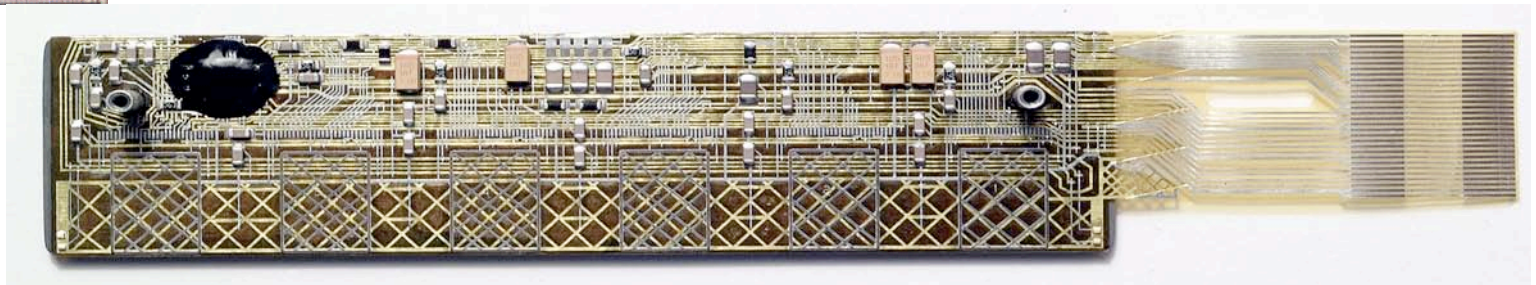
ALICE SDD FEE
Pascal chip:
64 channel preamp+ 256-deep analogue memory+ ADC
Ambra chip:
64 channel derandomizer chip

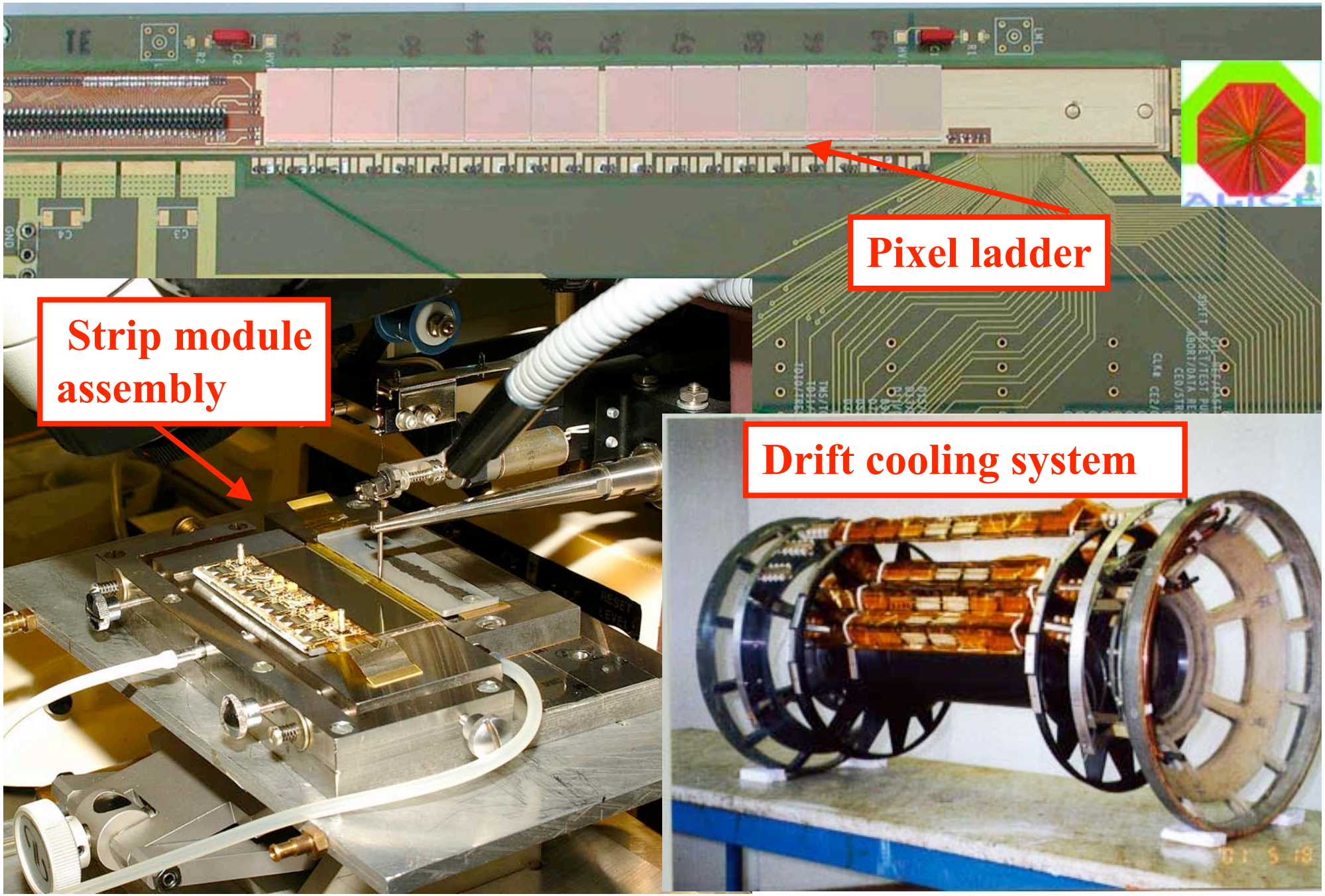




And extreme lightweight interconnection techniques:

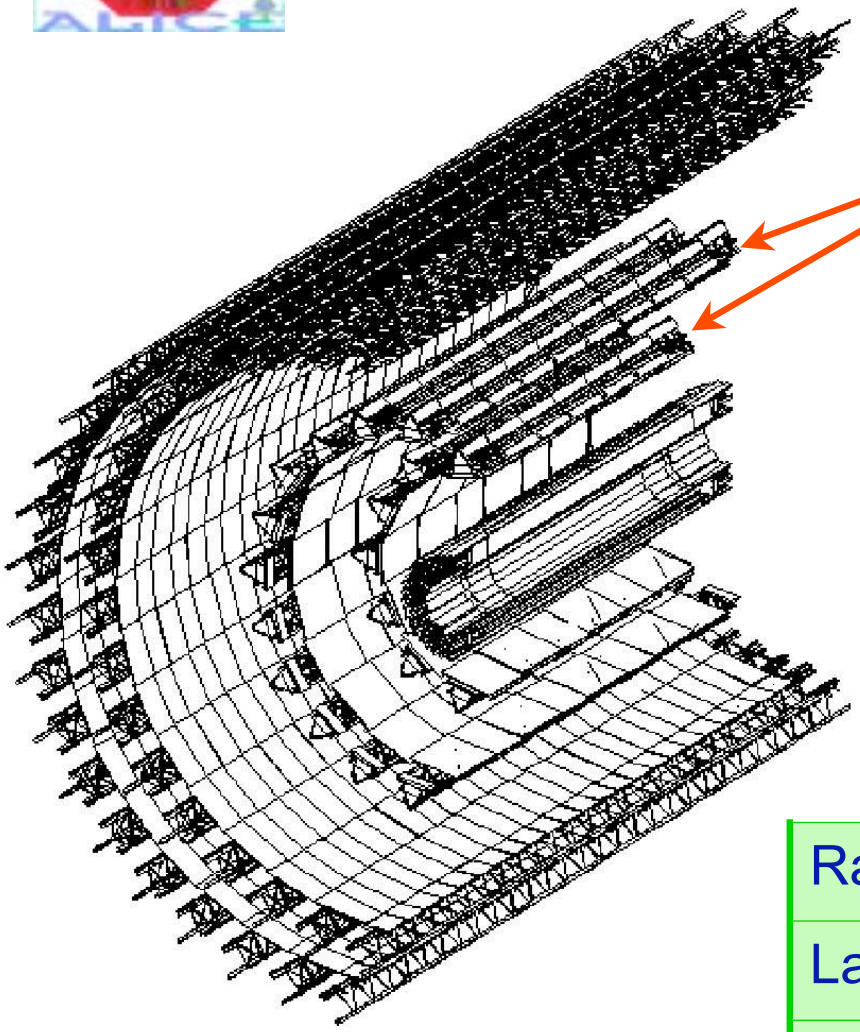
SSD tab-bondable Al hybrids





System testing and setting up of series production

SDD barrels



Silicon Drift Detectors

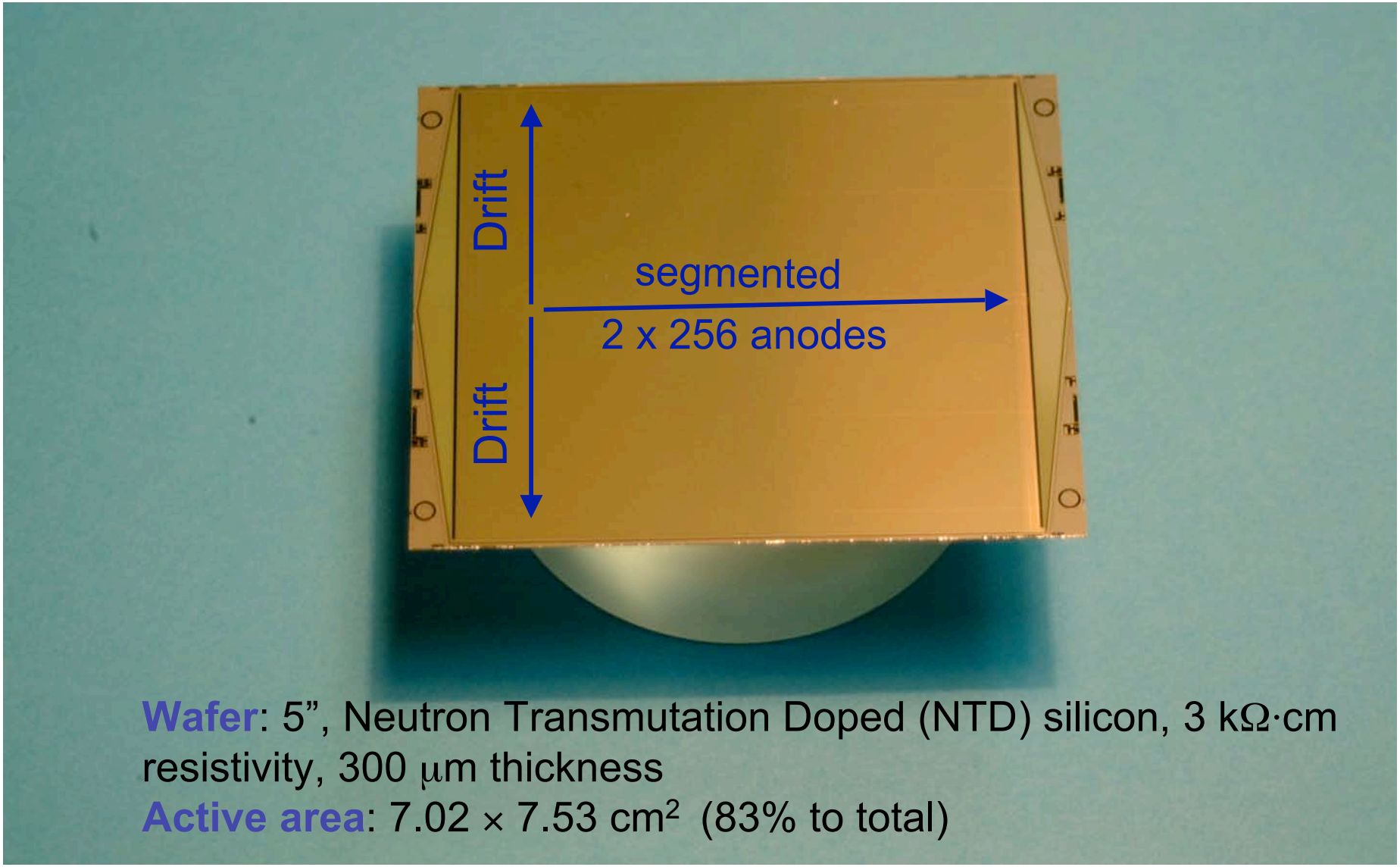
Tot. No. channels: 133 •10^3

Tot. No. detectors: 260

total area : 1.37 m^2

	Layer 3	Layer 4
Radius (cm)	14.9	23.8
Ladders	14	22
SDDs per ladder	6	8

ALICE Silicon Drift Detector



Wafer: 5”, Neutron Transmutation Doped (NTD) silicon, 3 kΩ·cm resistivity, 300 μm thickness

Active area: 7.02 × 7.53 cm^2 (83% to total)

SDD front-end and readout electronics

Design specifications

- dynamic range: up to 8 MIPs
- noise: 250 e^-
- readout time < 1ms
- power consumption: <5 mW/channel
- chips thinned to 150μm

PASCAL (64 channels)

- Preamplifier ($\tau \sim 40$ns, RC-CR^2 shaping)
- Analog memory (64 ×256 cells)
- 32 10-bit linear ADC (1 every 2 channels)

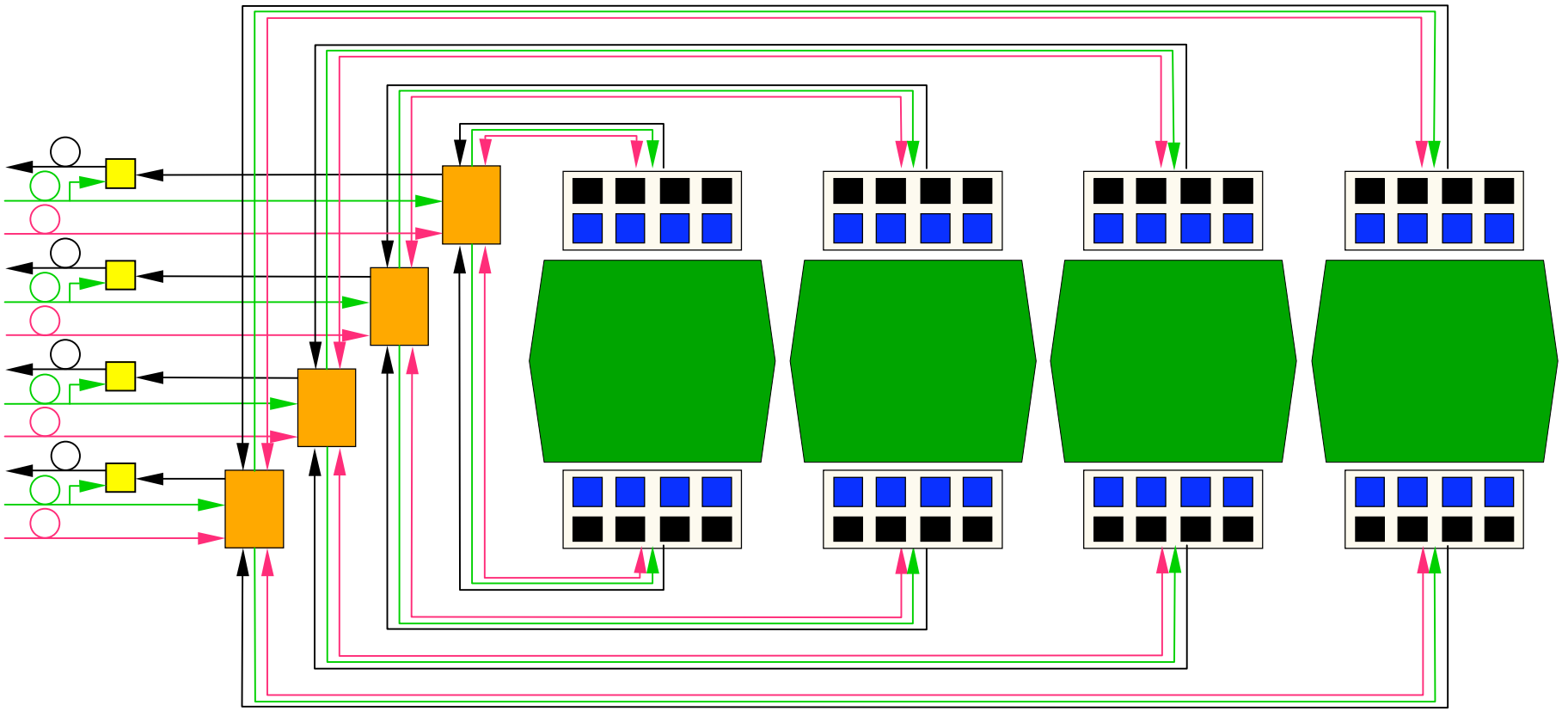
AMBRA (64 channels)

- Four 16 kB buffers
- Baseline equalization
- 10 to 8-bit compression

CARLOS (1 for 8 AMBRAs)

- Zero suppression and Compression of data from 1 SDD with a 2D – 2-Threshold algorithm (programmable parameters)
- Interface with AMBRAs, GOL and CARLOS-rx (FPGA based board, in counting room, which links to DDLs)
- FEE monitoring (SEU) time-multiplexed with data on the 16-bit output data bus
- Protections against radiation effects (parity check)

SDD readout architecture (each half-ladder)



PASCAL
AMBRA
CARLOS (data compression)
GOL (Gigabit Optical Link) + QPLL

40 MHz clock
Programming & monitoring
Data output & monitoring

Design of the 64-channel SDD hybrid