Mass production testing of the front-end ASICs for the ALICE SDD system

L. Toscano[a], R.Arteche Diaz[b,e], S.Di Liberto[b], M.I.Martínez[a,d], S.Martoiu[a], M.Masera[c], G.Mazza[a], M.A.Mazzoni[b], F.Meddi[b], A.Rivetti[a], F.Tosello[a], G.M.Urciuoli[b] and R.Wheadon[a]

for the ALICE collaboration

[a] INFN Sezione di Torino, via Pietro Giuria 1, 10125 Torino, Italy
[b] INFN Sezione di Roma, Piazzale Aldo Moro 2, 00185 Roma, Italy
[c]Dipartimento di Fisica Sperimentale, via Pietro Giuria 1, 10125 Torino Italy
[d] Instituto de Ciencias Nucleares – UNAM, Mexico City, Mexico
[e] CEADEN, Havana, Cuba
toscano@to.infn.it,

Abstract

The front-end system of the Silicon Drift Detector (SDD) to the ALICE experiment makes use of two Application Specific Integrated Circuits (ASICs). A total number of 4800 chips are employed to equip the two SDD barrels. This paper describes the test system developed for the wafer-level testing of the two ICs.

A dedicated setup has been designed to provide all the tests and to achieve a complete and efficient characterization for both chips, which are hosted on the same wafer. The two circuits (one mixed-mode and one fully digital) can be tested using the same apparatus with only small changes in the hardware.

Section I of the paper introduces the aspects of the SDD front-end electronics which are relevant to understand the rest of the presented material. Section II describes the architecture of the test system. The results of the tests and the selection criteria adopted for the chips are detailed in Section III and IV, respectively.

I. THE FRONT-END HYBRID

In ALICE (A Large Hadron Collider Experiment) [1,2], the Inner Tracking System (ITS) [3] is made up of six barrels of semiconductors detectors. The third and fourth ones will employ 260 Silicon Drift Detectors (SDDs) for a total sensitive area of 1.3m^2 [4]. The basic block of the SDD system is the module, which is composed of a drift detector, two front-end hybrids, flat signal/power cables, and electronic service cards which provide power regulation and digital signal buffering.

Each front-end hybrid processes the signals coming from half a detector (256 independent channels) and hosts four pairs of full-custom ASICs, named PASCAL (Preamplifier Analogue Storage and Conversion from Analogue to digitaL) [5] and AMBRA (A Multi-event Buffer Readout Architecture) [6]. A comprehensive description of the front-end architecture is provided in Ref. [7] and test results for the first front-end prototype are detailed in Ref. [8].

PASCAL is a mixed-mode integrated circuit that implements the amplification, analogue storage and analogue-to-digital conversion of signals coming from the anodes of the detector. This IC has 64 channels, each made of a low-noise amplifier and a 256 cells deep analogue memory formed by a switched capacitor array (SCA). When a trigger signal is received, the SCA is disconnected from the input amplifiers and its content is converted by a group of 10-bit successive approximation ADCs. For reasons of power consumption and space, there are only 32 ADCs, each one serving two contiguous channels (Fig.1). In order to allow optimisation of system readout time and performance according to different data-taking regimes, both the sampling frequency of the SCA and the conversion frequency of ADC can be programmed to work at the LHC clock frequency of 40MHz or to one half of it. At 40MHz, 256 μs are necessary to convert all the cells of the pipeline.

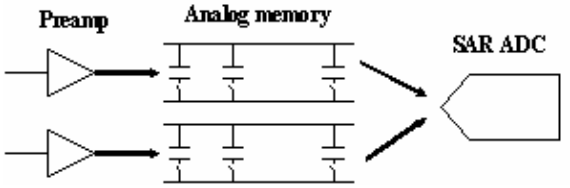

Figure 1: Schematic design of two contiguous odd and even channels in PASCAL

AMBRA is a control, pre-processing and buffering ASIC, which reads data from PASCAL on two 10 bit buses. The digitized data are pre-processed before storing them in one of the four 16 Kbytes RAMs. The first operation performed is the baseline equalization: a programmable 6-bit word for each of the PASCAL channels is subtracted from the corresponding input channel value. At this stage it is also possible to mask single defective channels. The second operation is a non-linear 10 to 8 bit digital compression. Finally data are stored in RAM adding a parity bit. Each AMBRA is designed to operate as one of four on a single hybrid sharing a single 9-bit output bus. With a 40MHz clock, the transmission takes 1.6 ms for a full event. During this phase AMBRA is still able to accept new triggers if at least one event buffer is free and PASCAL is not in the digitisation phase.

A single power bus line of 2.5V powers the front-end hybrid. To minimize switching noise generated during the operation of AMBRA it is important to separate power supplies and grounding for the two ASICs. For the same

reason the communication between the two chips occurs via low power differential transmitters and receivers. Finally, all communications between hybrid and the service electronics are based on standard LVDS transmitters and receivers with a nominal bus impedance of 100 Ω.

The two ASICs have been designed and produced in the same 0.25μm CMOS technology. Each 8-inch wafer hosts 146 potentially good pairs of PASCAL and AMBRA.

II. System architecture

The test system, shown in Fig.2, is based on a Cascade Microtech Rel-6100 probe station with a motorized chuck stage for 8-inch wafers controlled via GPIB interface.

The communication between AMBRA and PASCAL is based on LVDS drivers and receivers. To limit power consumption a resistive termination of 2kΩ (instead of 100Ω) was chosen and integrated as part of the receiver inputs of the chips. This change is possible because the transmission distance between AMBRA and PASCAL on the hybrid is very small, only 3mm. However this makes it necessary to use two active probe-cards (one per chip type) incorporating interface chips to convert the signals to standard LVDS. These buffers are located as close as possible to the probes in order to prevent reflections. Finally two full custom test boards are used to interface the probe cards with the logic analyser system. On these boards, commercial LVDS receivers accept differential input signals from the probe card and translate them to 3.3V CMOS outputs levels. The drivers accept 3.3V CMOS input from the logic analyser and translate them to LVDS signals. The rest of the testing infrastructure is common to both ICs.

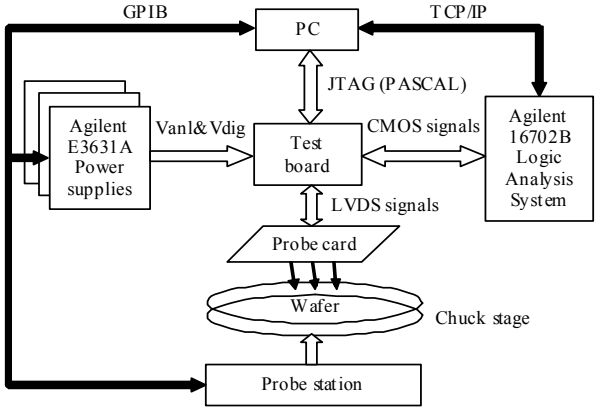

Figure 2: Schematic design of the on-wafer test system set-up

Three Agilent E3631A power supplies controlled through the GPIB bus are used to provide power to PASCAL (with separate analogue and digital supplies), AMBRA, test boards and probe cards. This system also provides the measurement of the power consumption of each chip, by measuring the current of the different channels via GPIB.

A data pattern generator creates the digital control signals for the characterization of the two chips. The outputs are read out by the logic state analyser on the same instrument (Agilent 16702B Logic Analysis System). All outputs are transmitted to a PC via TCP/IP. The test of PASCAL requires an intensive use of the JTAG port of the chip. However, since uploading the data patterns used to implement each JTAG command to the pattern generator requires few seconds, it was chosen to implement a separate JTAG interface using the parallel port of the PC.

The test system is controlled by a PC running dedicated software developed in LabVIEW. Two front panels (one for AMBRA and one for PASCAL) allow the user to configure the test procedures. The program executes automatically all the measurements and performs online the data analysis. After the analysis, the results of the tests are stored in the production database, which serves to select the good dies to be mounted in the system.

To build layer three and four of the ITS a total number of 260 (84+176 respectively) SDD modules are required. Having two front-end hybrids per module implies a total number of 2080 for both AMBRA and PASCAL. Taking into consideration a number of spare chips of 15%, 4800 good chips are needed. The time necessary for the characterization of a single chip is 220 seconds for AMBRA and 510 seconds for PASCAL.

III. Test procedures and test results

The AMBRA chips are selected performing on each die a set of four different tests. These measurements allow assessing the performance of the various part of the IC, by checking in detail the memory buffers, the internal registers and the control logic. Since AMBRA is a pure digital chip, the data analysis mainly consists in comparing the output digital streams with the expected ones. This comparison can be carried out efficiently by the internal software of the logic state analyser, and for maximum speed only the errors are then transferred to the computer. PASCAL demands instead a more sophisticated data analysis, which is necessary to evaluate the quality of the analogue parts of the chip. In this case the raw data are sent directly to the PC, which run online the routines to extract the relevant parameters (e.g. noise and gain for each channel, linearity, etc).

A. AMBRA power consumption test

The first test performed checks the power consumption: the test system measures the AMBRA core current (I_{dd}) and the pad drivers current (I_{dde}) at 40MHz checking if they are within the range of acceptance. The value of I_{dd} must be within 40 mA and 50 mA and the one of I_{dde} has to be between 30 mA and 40 mA. Fig.3 and Fig.4 show as example values of good AMBRA chips on one wafer (SK8MQHX).

B. AMBRA Functional tests

The AMBRA functionality is tested at 40 MHz with four different test benches. Each test bench contains between 30k and 50k test vectors.

The first test bench checks the basic functionality of the chip and the I/O interfaces. It is a first-level check that allows

to discard immediately the highly defective chips (i.e. defective pad drivers, faults in the control units, etc.).

The second test bench is dedicated to the check of the baseline subtraction logic and the data compression circuitry. A full scan of the 1024 possible input values and the corresponding 256 output values is performed.

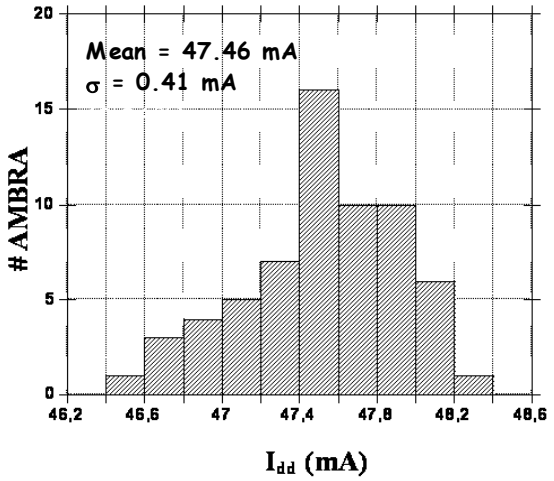

Figure 3: I_{dd} values of good AMBRA chips on wafer SK8MQHX. Acceptance range : between 40 mA and 50 mA

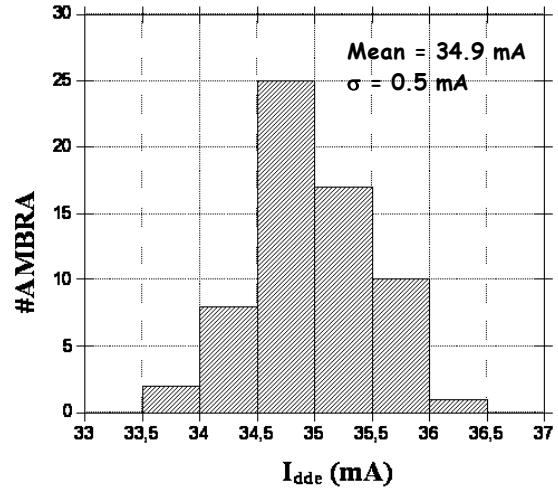

Figure 4: I_{dde} values of good AMBRA chips on wafer SK8MQHX. Acceptance range : between 30 mA and 40 mA

The third test makes a full check of the memory buffers; each bit of the four 16Kx9 memories is written with a logic 0 and a logic 1 in order to detect a possible failure in the memory cell. The pattern used for the test is an alternate sequence of '0's and '1's, in such a way that each memory cell has its four neighbours in the memory matrix written with the opposite logic value. This method is used to take into account proximity effects on cells with open circuit failures. In order to check all possible combinations, three full write/read cycles are necessary: one with the alternate sequence of '0's and '1's, the second with its binary complement and the third with an odd number of '1's to complete the test for the parity bit.

The fourth test bench is dedicated to the JTAG interface. All the JTAG configuration registers are written and then readout with the same bit patterns used for the memory. In this test the functionality of the addressing protocol used to send JTAG commands on a specific chip (named ASP and described in [6]) is also tested.

C. PASCAL tests

The PASCAL test procedure consists of a set of six single tests: power consumption, ADC full/half frequency mode, analogue memory full/half frequency mode, noise, baseline and linearity.

The power consumption test measures the current of the power supply pins that are grouped in three categories: I_{ADC} is the ADC current, I_{anlg} is the analogue current and I_{dig} is the digital current. The system tests the values from PASCAL and compares them with two thresholds, first without clocking the digital part and then after clocking it at 40MHz. The test is passed if the value is in the range defined by the two thresholds. As expected, the values of I_{ADC} and I_{anlg} are not sensitive to the clock (Fig.5 shows an example for the ADC current) while there is a significant increment of the digital current values due to the switching of the CMOS logic (Fig.6).

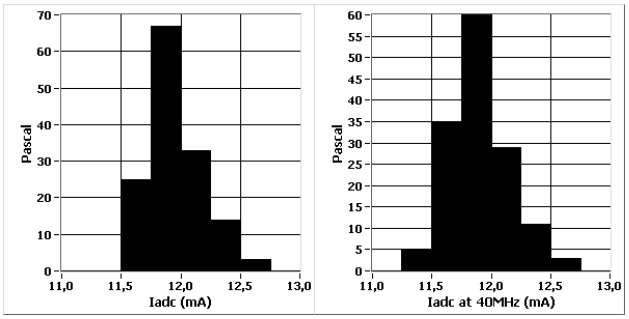

Figure 5: ADC current without clock and at 40MHz measured for 143 PASCAL chips in wafer ALEQARX. The mean value is about 11.9 mA in both cases. Acceptance range: between 11mA and 13mA

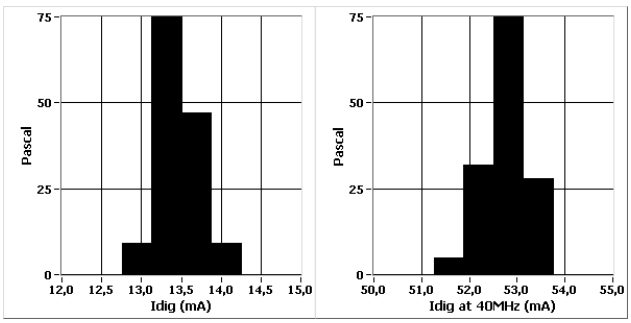

Figure 6: Digital current without clock and at 40MHz measured for 143 PASCAL chips in wafer ALEQARX. The mean values are: I_{dig} (no clock) = 13.5 mA, I_{dig} (40MHz)= 52.5mA. A variation of 10% around the mean values is acceptable in both cases

The ADC full/half frequency mode test programs via JTAG the frequency for the analogue to digital converter, which can work with a 40MHz or a 20MHz clock. Since the digital current consumption of the chip is reduced when the ADC operates at 20MHz, the current consumption at 20 MHz

is compared to the one at full frequency to detect if the command has been correctly interpreted.

The analogue memory full/half frequency mode test checks if the analogue pipeline can be programmed correctly via JTAG to work at half the sampling frequency. In some experimental conditions, in fact, it will be necessary to reduce the amount of data to be digitized and transferred in order to cope with higher trigger rates. The reduction of the sampling frequency by a factor of two halves the number of samples for a given drift time of the detector, while leading to an acceptable decrease in resolution. This test is done by using the internal test pulse generator. PASCAL is equipped with a system that allows generating a programmable voltage step which is fed through calibration capacitors to the input of each preamplifier. The calibration circuit delivers input signals up to a maximum of 32 fC with a step of 0.06 fC.

In this test a fixed signal of 20 fC is injected in all the channels. The outputs of the amplifiers are sampled by the pipeline. If all the other conditions are not changed, the position of the sampled signal stored in the pipeline is shifted in a predictable manner when the sampling clock is modified. Hence, by changing the sampling frequency from 40MHz to 20 MHz it is possible to measure if the position of the test signal moves as expected.

After the chip has passed the functional tests, a set of three measurements is run to check the performance of the analogue blocks.

The noise test measures the rms noise of each of the 64 channels. The experimental conditions do not allow reaching the same level of noise obtained when the chip is mounted on the hybrid. For the same bias settings, the noise is 1.6 ADC count rms (corresponding to an ENC of 320 electrons) on the hybrid and 4 ADC counts rms (800 electrons) on the probe station. The difference is primarily due to the fact that on the probe cards the filtering capacitors can not be placed as close to the chip as in the final set-up. This determines a non-optimal filtering of the power supplies and, more important, of the Low-Dropout Regulators integrated on chip that provides the reference voltage to the ADCs. The noise test proved nevertheless to be useful in a prompt identification of defective channels.

The scope of the baseline test is to verify if the 9-bit DAC that sets the value of the DC voltage at the output of the front-end amplifier works properly. This component has been extensively characterized during the prototyping phase. In the mass production testing it is not possible to check all the possible patterns because this would make the duration of the measurement prohibitively long. Hence the test is performed by using a set of nine different test vectors that check that all the individual bits switch as expected. A linear fit to the data allows then to calculate the gain of the DAC. The theoretical value of the slope obtained in this manner is expected to be 0.95 and values between 0.9 and 1 are considered acceptable, since they are consistent with the tolerance of the process. The result of this test done on 31744 channels of chips coming from four different wafers has given 27743 channels in range (Fig.7).

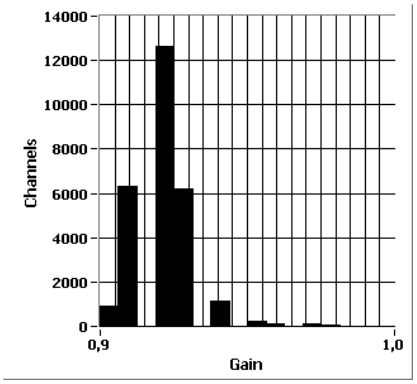

Figure 7: Baseline gain values. A total number of 27743 channels have been considered in this plot.

The linearity test employs the test pulse generator embedded on chip to evaluate the gain and the linearity of the whole chain. Nine different incremental signals are injected. The step between the signals is not uniform, but it is chosen to explore in more detail the lower part of the dynamic range. Fig.8 shows gain values of 29055 good channels from 496 different chips in 4 different wafers. Due to the spread of the process parameters a variation of the gain of 10% around the nominal value (45mV/fC) is expected and is consistent with the measured data. It must be pointed-out, however, that the gain uniformity on the same chip is usually better than 1%.

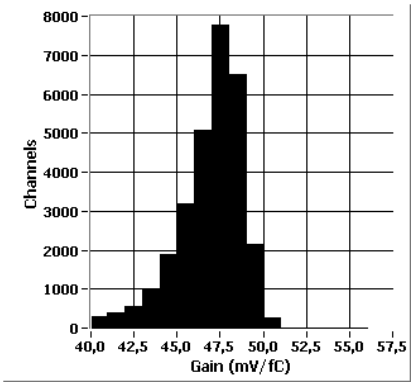

Figure 8: Gain distribution for PASCAL. The result is obtained on 29055 channels. Acceptance range: from 40 mV/fC to 50 mV/fC.

IV. CHIP SELECTION CRITERIA

As described above, to calculate the yield for both ASICs selection criteria have been defined considering the power consumption measurements and the results of the detailed tests.

The AMBRA chips are grouped in the following classes:

- Class A (“good”) if the power consumption test and all the functional tests are passed without errors;
- Class B (“grey”) if power consumption, JTAG and control logic test bench are passed without errors and no more than 128 memory bits in the RAMs are defective;
- Class C (“bad”) all the other ones.

The PASCAL ICs are grouped as following:

- Class A ("good") if all the six tests are passed without errors;
- Class B ("grey") if the first three tests are passed and at least one of the last three fails. This class includes circuits that are fully functional at the logic level but exhibit at least one dead or noisy channel;
- Class C ("bad") if any of the first three tests is fails.

To build the front-end hybrids only Class A chips are used. Class B will be used only if the yield of the hybrid and the module construction will be too low. Tab.2 and 3 show the yield figure for AMBRA and PASCAL, respectively. These results have been obtained on 7 wafers, coming from two different batches. The fraction of Class A chips is 84.1% PASCAL and 71.6% for AMBRA.

V. Conclusions

A test system for the mass production testing for the front-end ASICs for ALICE SDD system has been designed and built. The system is based on a commercial data pattern/logic state analyser mainframe. The apparatus allows the characterization of two different integrated circuits hosted on the same wafer with small changes in the testing hardware. The equipment is supervised by dedicated software in LabVIEW that controls all the operation and performs on line the data analysis necessary for the selection of the components. The time required for testing one IC is 510 seconds for PASCAL and 220 seconds for AMBRA.

Both chips are tested in detail on wafer at the nominal working frequency of 40 MHz. Depending on the results of the tests each die is assigned to one of three classes. Only Class A chips that meet the most stringent selection criteria will be mounted on the ITS.

Considering the first 7 wafers tested, 84.1% of "Good" PASCAL chips and 71.6% of "Good" AMBRA chips were obtained. The lower yield of AMBRA can be explained with the fact that this ASIC has a much higher number of transistors. The yield figures found are however satisfactory and will allow to have in due time all the chips needed for the construction of the SDD barrels.

Table 1: First 7 wafers tested for PASCAL chips. 84.1% chips are "Good", 10.4% are "Grey" and 5.5% are "Bad"

	Wafer	Meas	Class A	Class B	Class C
Eng. Run	EB4GADX	147	121	18	8
	EM4GC1X	142	125	14	3
Prod. Run	SK8MQHX	131	94	28	9
	AXEQFNX	147	119	15	13
	AWEQ9ZX	145	125	14	6
	ASEQAKX	147	134	8	5
	ATEQAJX	146	127	8	11
	Total	1005	845	105	55

Table 2: First 7 wafers tested for AMBRA chips. 71.6% chips are "Good", 7.4% are "Grey" and 21% are "Bad"

	Wafer	Meas	Class A	Class B	Class C
Eng. Run	EB4GADX	151	115	8	28
	EM4GC1X	150	129	10	11
Prod. Run	SK8MQHX	147	63	21	63
	AXEQFNX	151	114	13	24
	AWEQ9ZX	151	109	10	32
	ASEQAKX	150	110	9	31
	ATEQAJX	151	113	7	31
	Total	1051	753	78	220

VI. References

[1] The ALICE collaboration, ALICE Technical Proposal, CERN/LHCC, 95-71, December 1995.

[2] The ALICE collaboration, Technical Design Report of the Inner Tracking System, CERN/LHCC, 99-12, June 1999, pp. 83-173.

[3] F. Tosello, Nucl. Instr. And Meth. A 473 (2001) 210.

[4] A. Rashevsky, et al., Nucl. Instr. And Meth. A 485 (2003) 640.

[5] A. Rivetti, et al., The front-end chip for the silicon drift detectors of ALICE, INFN Internal Document, online: www.to.infn.it/~vlsi, May 2004.

[6] G. Mazza, AMBRA: a multi event buffer readout architecture for the SDD system of the ALICE experiment, INFN Internal Document, online: www.to.infn.it/~vlsi.

[7] A. Rivetti, et al., Nucl. Instr. And Meth. A 485 (2002) 188.

[8] A. Rivetti, et al., Nucl. Instr. And Meth. A 541 (2005) 267.