PIXEL2000, June 5-8, 2000

STATUS OF THE ALICE PIXEL DEVELOPMENTS

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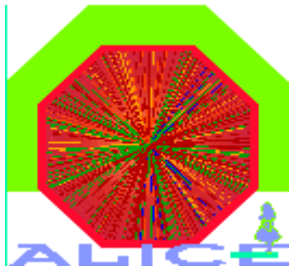
For the ALICE Collaboration



CONTENTS:

- Introduction:
  - Physics Requirements
  - Design Considerations
- Present development status and related issues:
  - Front-end chip
  - Ladder & stave layout
  - Read-out & control
  - Global layout

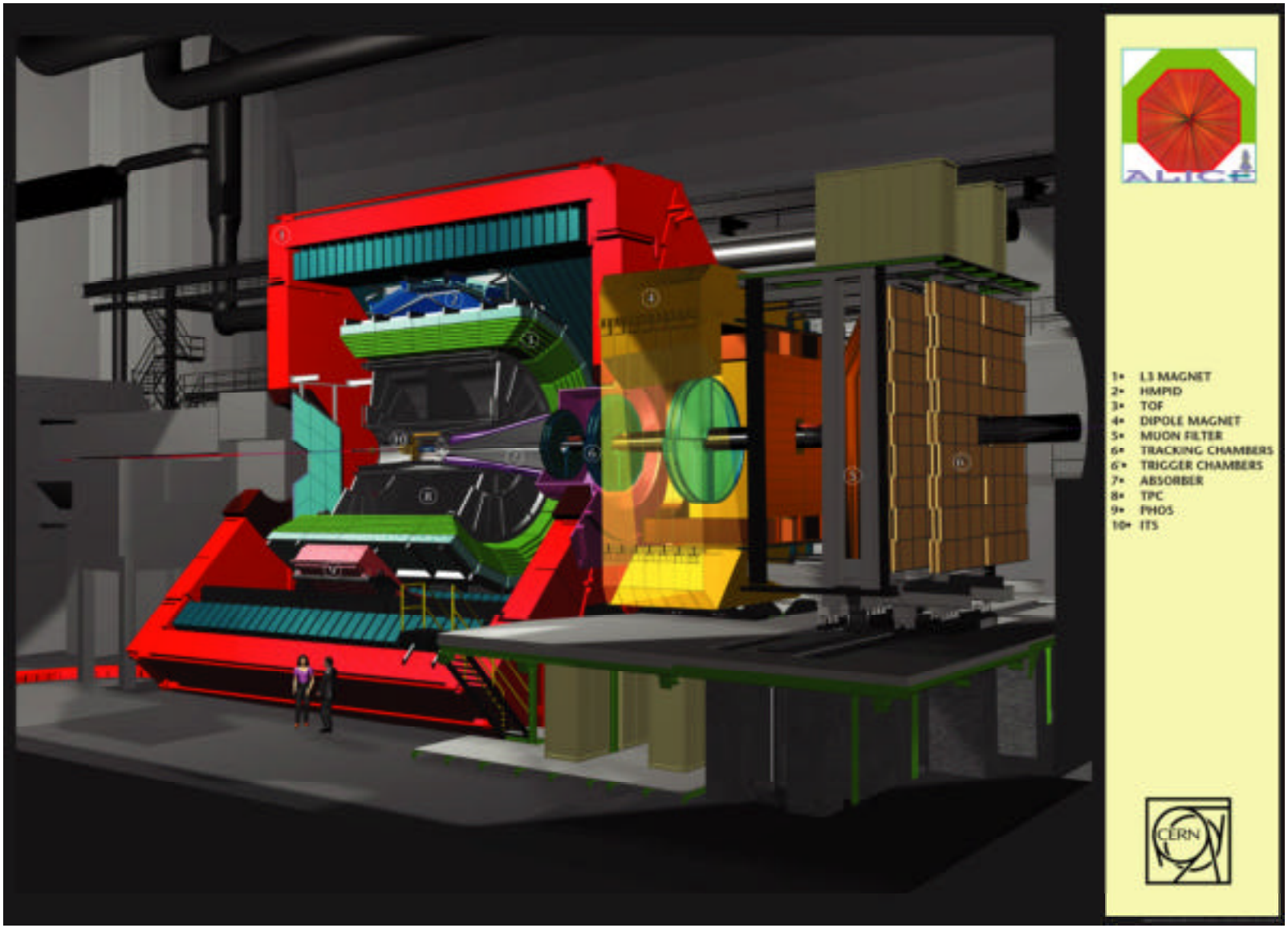
Institutes that will construct and operate the ALICE-ITS-PIXEL

- CERN
- ITALY

Bari (INFN,University and Politecnico)
Catania (INFN and University)
Legnaro (LNL-INFN)
Padova (INFN and University)
Roma (INFN and University)
Salerno (INFN and University)

- SLOVAKIA

Kosice (Institute of Experimental Physics,
Slovak Academy of Sciences and
Faculty of Science P.J. Safarik University)


ALICE
1• L3 MAGNET
2• HMPID
3• TOF
4• DIPOLE MAGNET
5• MUON FILTER
6• TRACKING CHAMBERS
6'• TRIGGER CHAMBERS
7• ABSORBER
8• TPC
9• PHOS
10• ITS
CERN

ALICE SPD AS PART OF CENTRAL TRACKING SYSTEM: REQUIREMENTS

- Determination of secondary vertices:

Charm & Beauty decays study

⇒ Impact parameter resolution needed $\sigma(r\varphi) <\sim 50\ \mu m$

- Central Pb-Pb collisions: High track densities ($> 50\ cm^{-2}$)

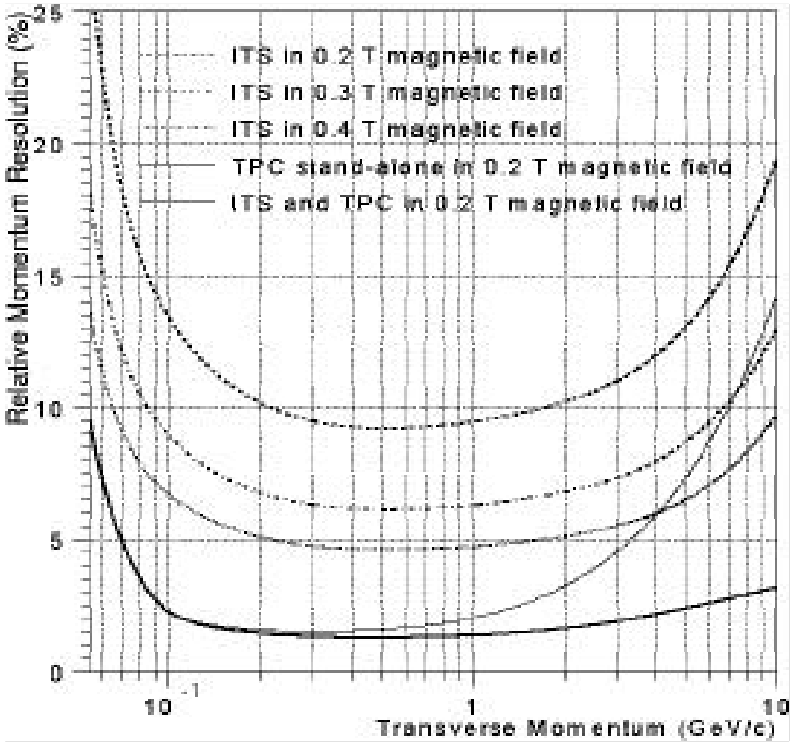
⇒ Need high resolution & high granularity:

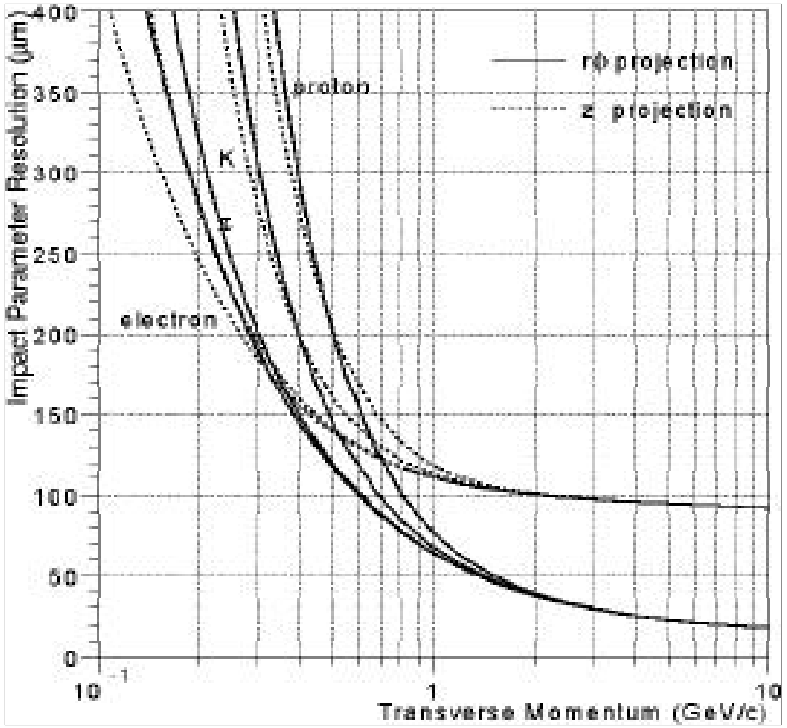
Two SPD Layers at 4 cm & 7 cm from beams
with acceptance of $\pm 45°(\theta)$ $[|\eta| < 0.88]$
for vertices within the length of the interaction diamond
SPD with cell size: 50 μm ($r\varphi$) & 425 μm (z)

ALICE: WHOLE ITS & TPC
SIMULATION

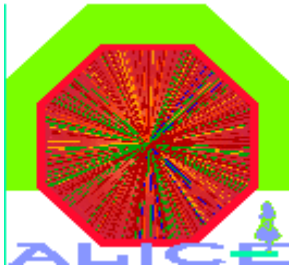
Tracking precision: 12 μm (rφ) & 100 μm (z)

Two tracks separation: 100 850





Impact parameter resolution:
50 μm (rφ) @ pt = 1.3 GeV/c



ALICE SPD AS PART OF DIMUON SPECTROMETER: REQUIREMENTS

- Determination of primary vertices for the dimuon physics

  Vertex position bounded by the vertex diamond
  Size of the bunch: $\sigma x = \sigma y = 15 \mu m$ & $\sigma z = 5.3 cm$

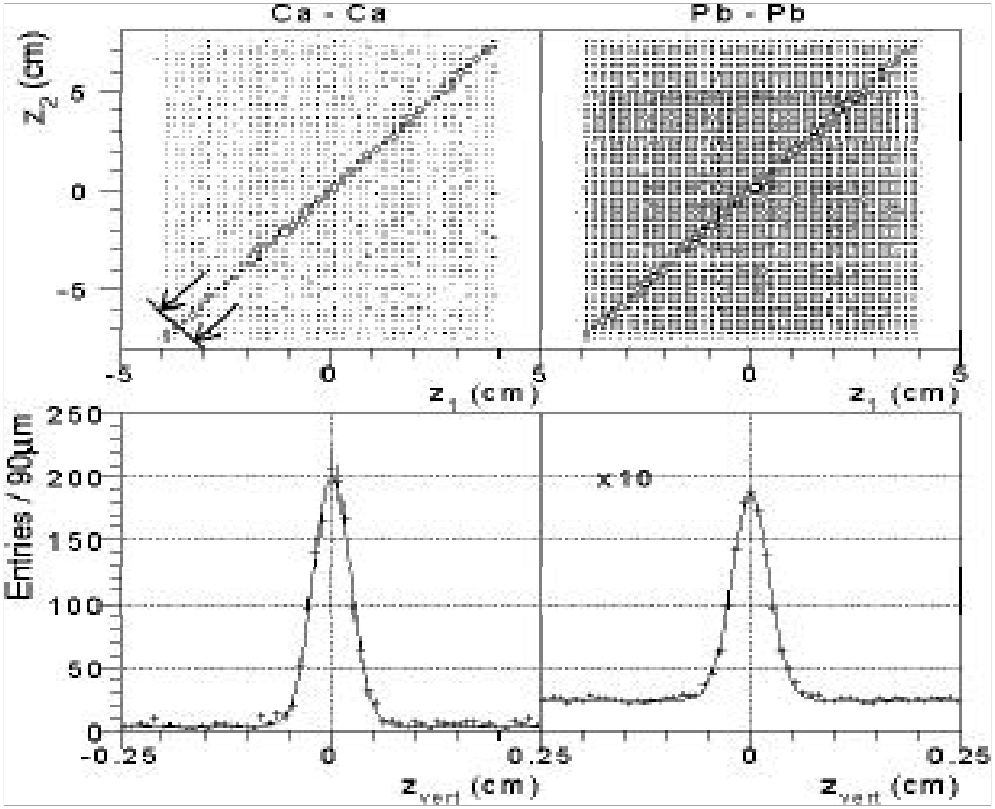
  → Primary vertex resolution needed: few ~ 10 μm

- Read-out capability during high-L run with muon arm

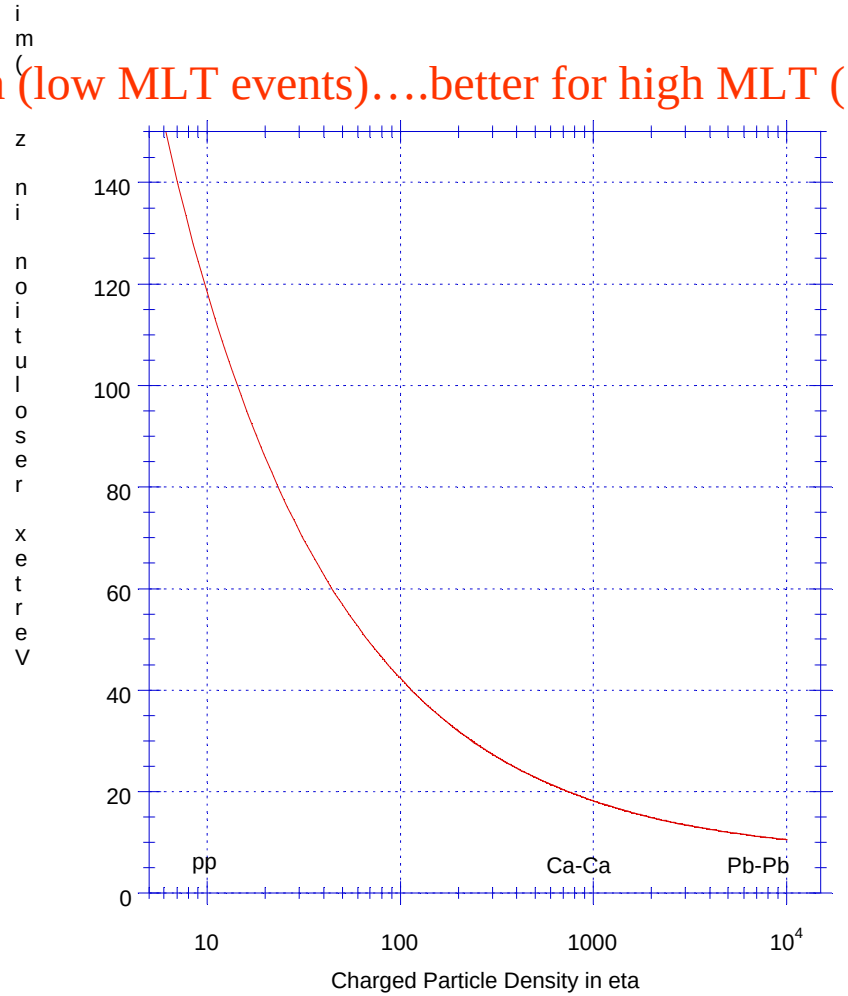
  → SPD higher rate central tracking device

ALICE SPD STANDALONE PRIMARY VERTEX RESOLUTION (Z): SIMULATION

$\sigma(r\varphi) < 10\ \mu m$ & $\sigma(z) < 15\ \mu m$ (low MLT events)….better for high MLT (!)



Correlation of the hits in the two pixel layers



Resolution of the vertex along z-axis

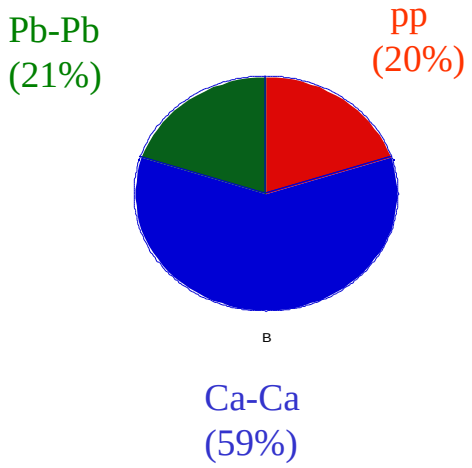
ALICE SPD RADIATION TORERANCE REQUIREMENTS

R (cm)	*± Z (cm)*	*Area (m^2)*	*Charged Particles Density in central Pb-Pb (cm^{-2})*	*Occupancy (%)*
4	28.3	0.077	89	2.1
7	28.3	0.154	22	0.6

- At r ~ 4cm during a running period of 10 years:

Total DOSE = 130Krad (1,3KGy)

Specification: ~ 500Krad (50KGy)



Total neutron flux < 10^{12} cm^{-2}

ALICE SPD: The ALICE1 chip

FRONT-END CELL: "EDGELESS" DESIGN in 0.25 μm CMOS technology
Chip size ~ 15 mm x 14 mm & Total # transistors ~ 13 Million
RADIATION TOLERANCE issue:
tests done by X, γ rays & protons on Alice2Test chip
→ It survives up to 30 Mrad

Main specifications:

Cell size	50 μm ($r\phi$) × 425 μm (z)
Number of cells	256 ($r\phi$) × 32 (z)
Minimum threshold	below 2000 e-
Threshold uniformity	200 e-
Strobe (LVL1) latency	up to 10 μs
Strobe duration	200 ns
Clock frequency	10 MHz

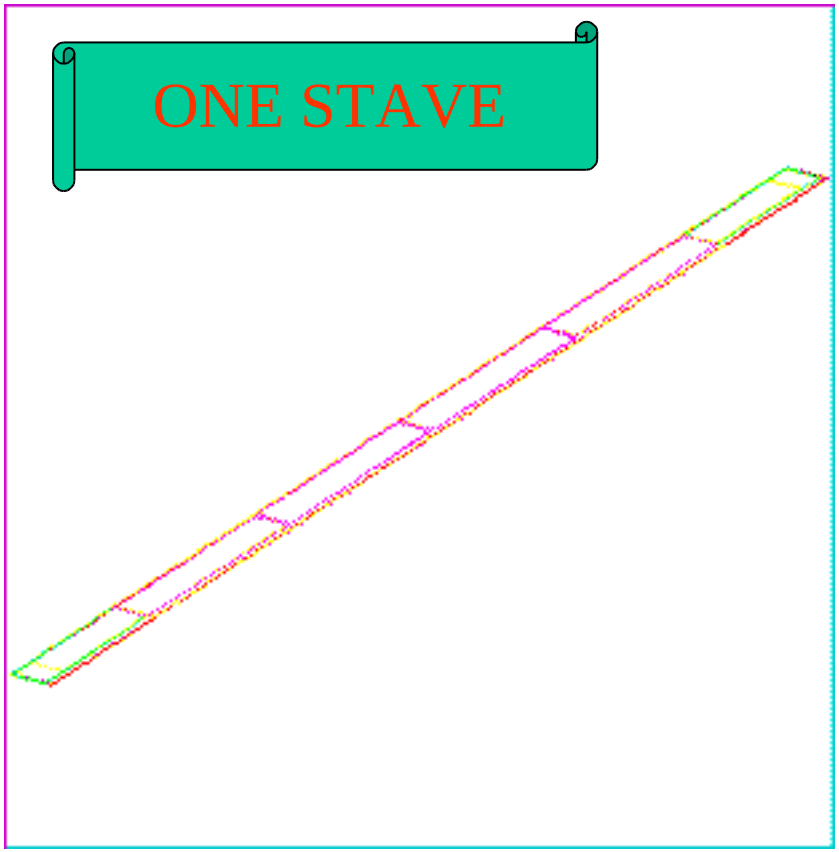
Robustness:
- Individual cell threshold adjust (3bits)
- Individual cell mask
- Digital bias adjust
- JTAG controls

Status: Submitted to IBM
→ Expected back in July

ALICE SPD: ASSEMBLY OF R-O CHIPS

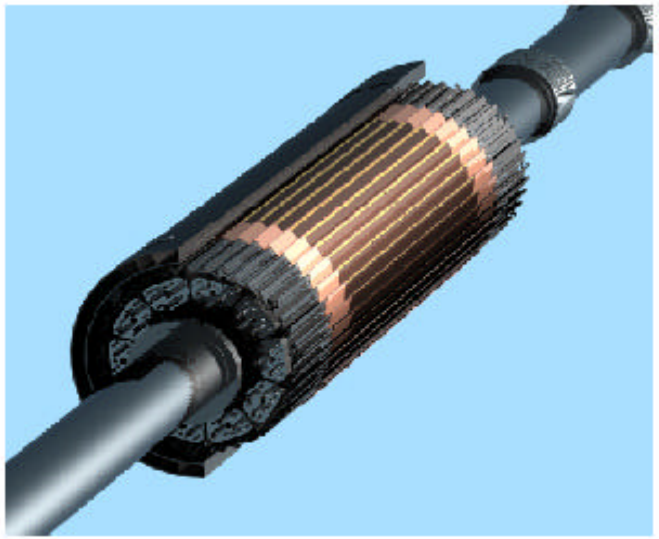
one-LADDER:
high resistivity silicon matrix
bump bonded to 5 read-out chips
("hybrid" technique)
half-STAVE:
two ladders
(10 r-o chips ~ 82k pixels)
+ one pilot chip
+ one optical link
+ timing & control interface

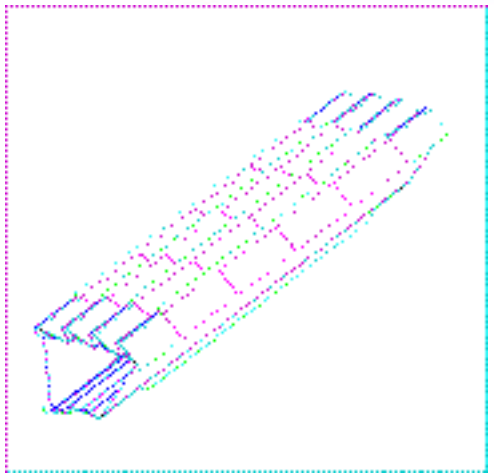
ONE STAVE

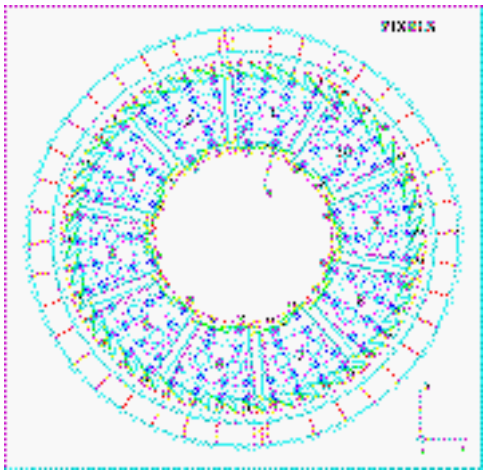


ALICE SPD: GLOBAL LAYOUT

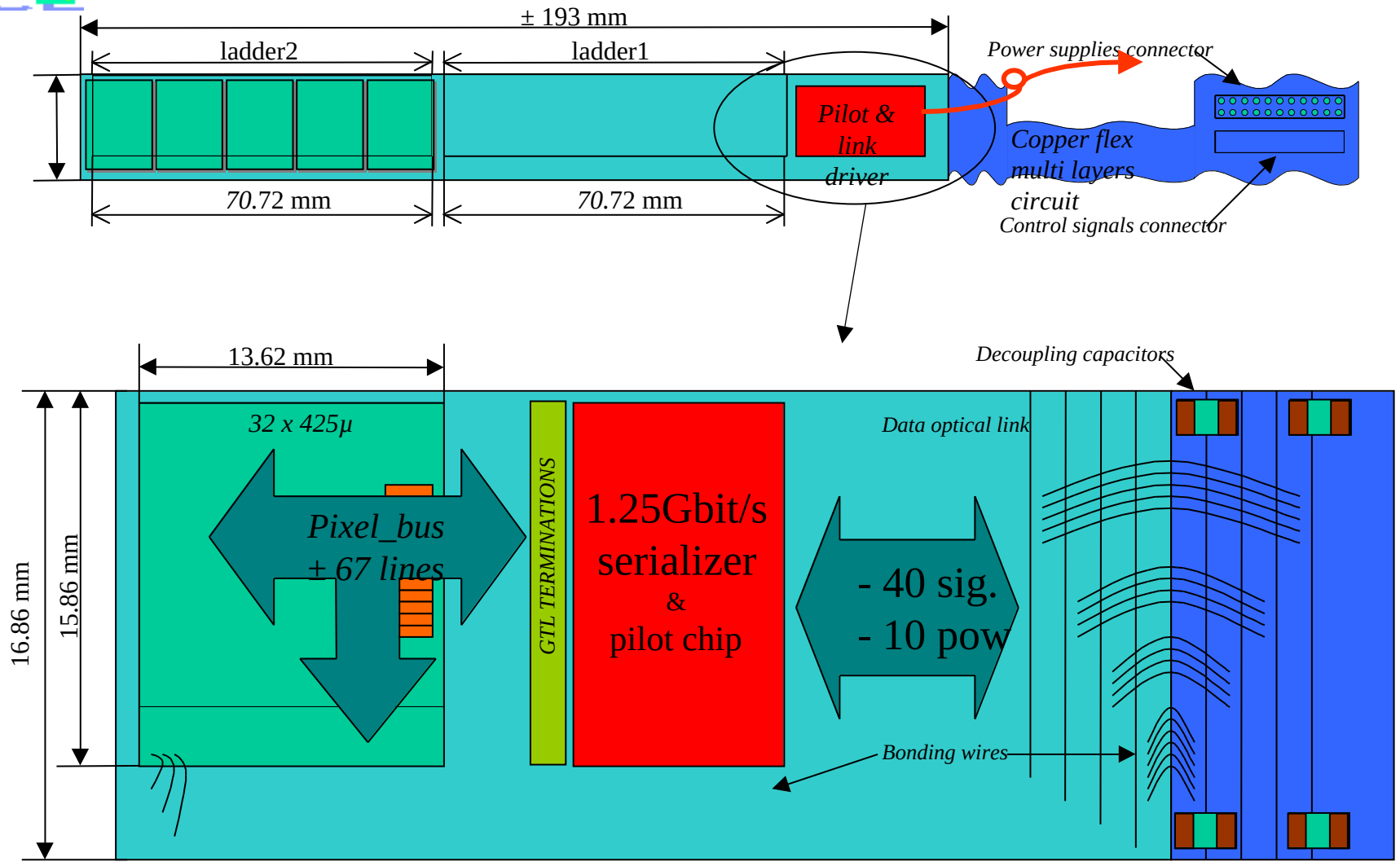
10 carbon-fibre support sectors
6 staves per sector
(2 from inner
4 from outer layer)
In total:
60 staves
240 ladders
1200 chips
9.8 M pixel cells



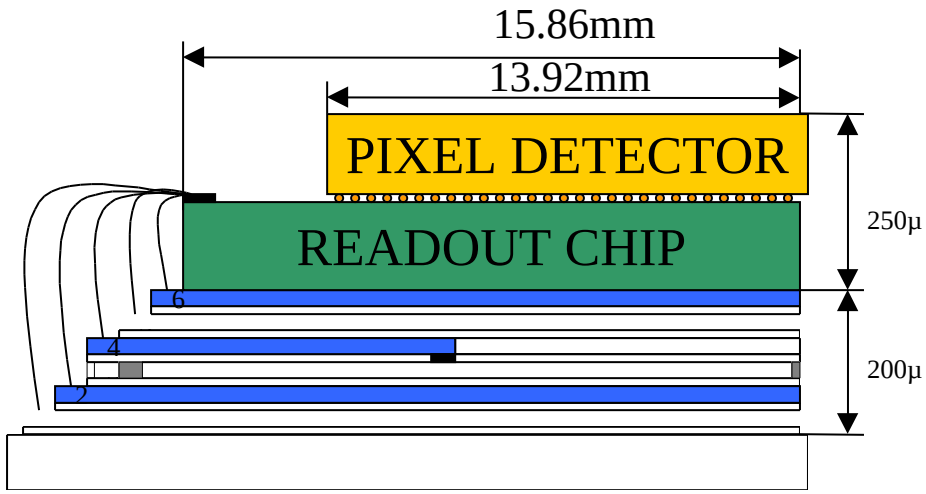


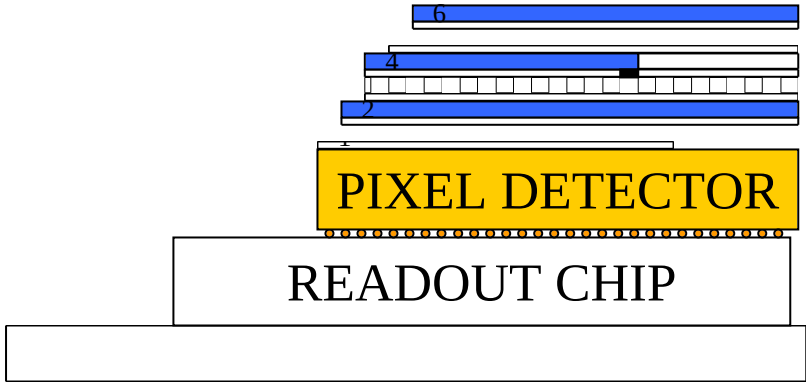


ALICE SPD: PIXEL BUS ISSUE



ALICE SPD: TWO PIXEL BUS HYPOTHESIS





Via between horizontal and vertical lines

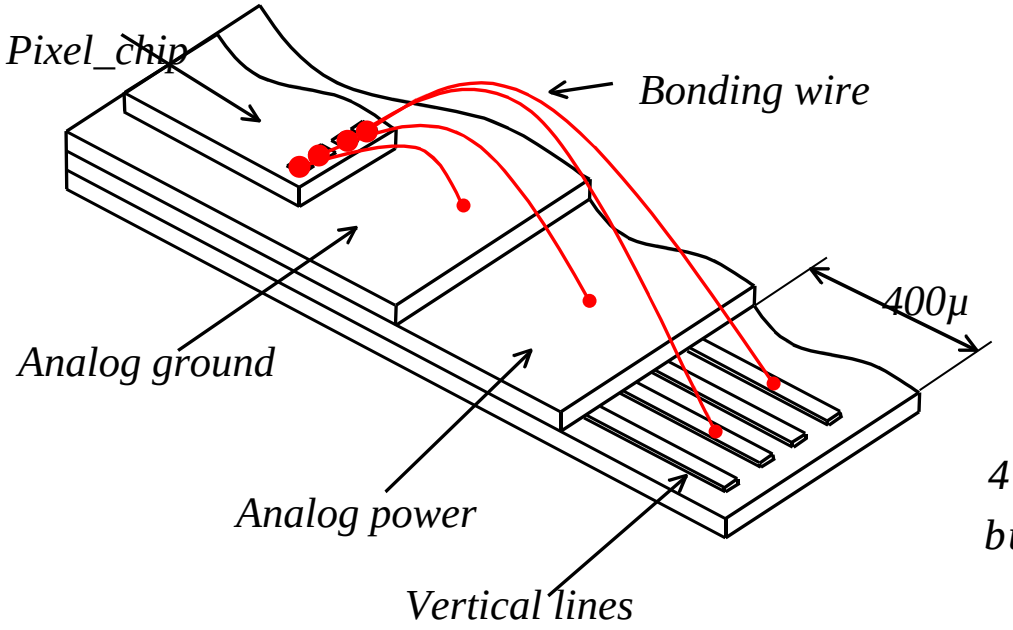
Aluminium

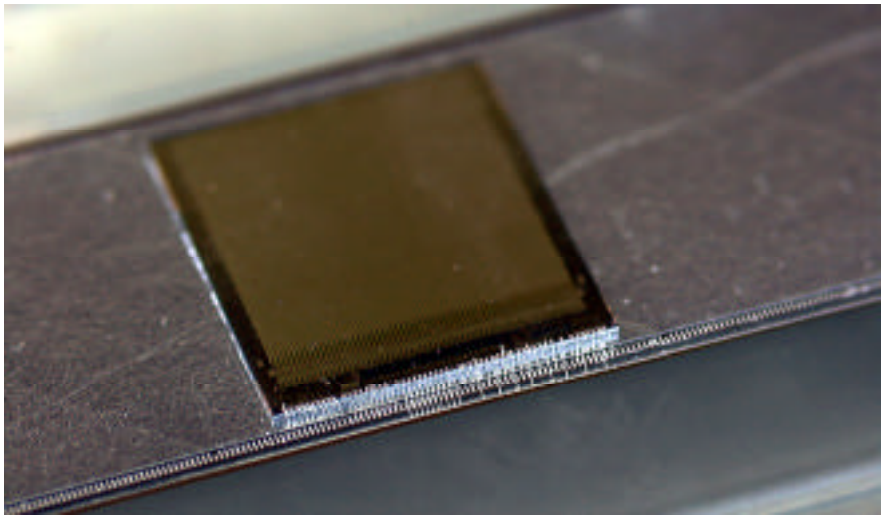
Solution A ***Solution B***

Each one has pros and cons: more studies are needed to decide

ALICE SPD: MULTI LAYERS BONDING CONNECTIONS ISSUE

1-st essay . . . .





200mm x 17mm
4 aluminium layers
bus = 81 lines 100µ

Aluminium: 15µ
Kapton: 50µ
Glue: 10µ
Total thickness:300µ

. . .mechanically it's feasible! → Next step: 200µm & 6 Al layers

ALICE SPD: HALF STAVE R/O & CONTROL

PILOT CHIP: same technology as for front-end chip (0.25 μm "rad.tol.")

→ **SLOW CONTROL**:

boundary scan, parameter loading (JTAG standard)

→ **TRIGGER DISTRIBUTION**:

LVL1 (5.5 μs) , BUSY

LVL2Y (100 μs), LVL2N (< 100 μs)

10 chips x 256 clock cycles @ 10 MHz (256 μs)

→ **READOUT CONTROL OF FRONT-END CHIPS**

ROW DATA SERIALIZATION AND TRANSMISSION OFF-BARREL

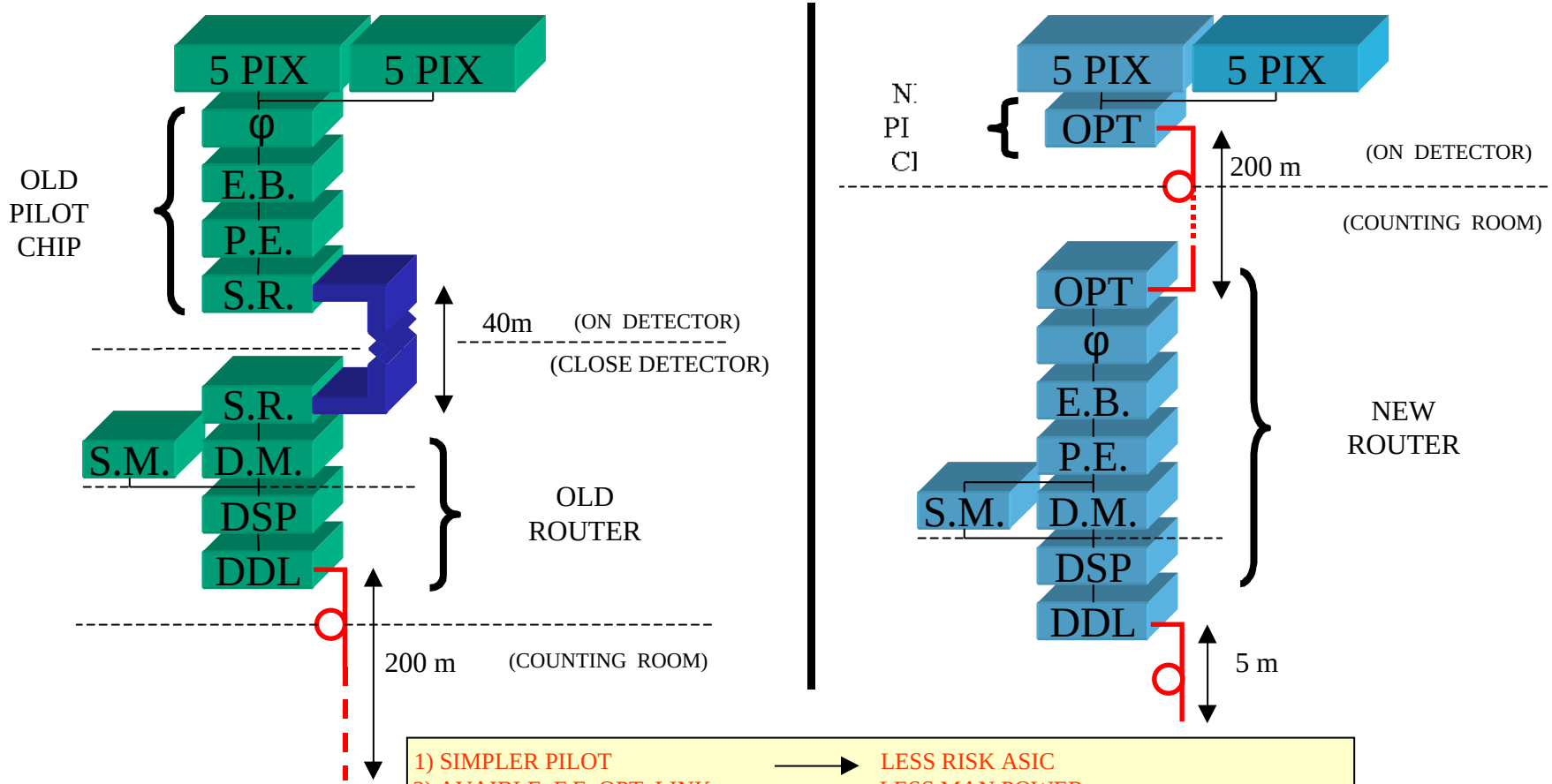
zero-suppression & hit encoding done on ROUTER VME board (located in c.r.)

→ CENTRAL Pb-Pb EVENT DATA SIZE:

~ 400kbyte/event

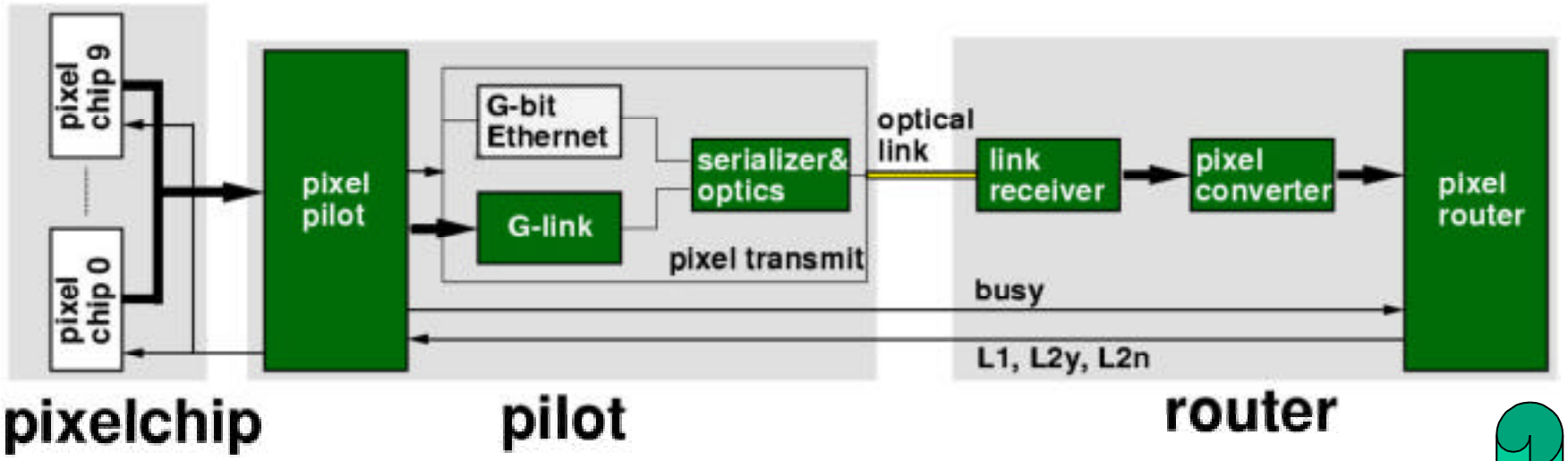
(50% data reduction formatting data possible, but loss of redundancy!)

ALICE SPD: GLOBAL READ-OUT ARCHITECTURE (BLOCK DIAGRAM)



1) SIMPLER PILOT	→	LESS RISK ASIC
2) AVAIBLE F.E. OPT. LINK	→	LESS MAN POWER
3) 200 m LINK	→	ROUTER ACCESSIBLE
4) FPGA + MEM + DSP ROUTER	→	FLEXIBILITY FOR FUTURE "UPGRADINGS"
5) RAW DATA TRANSMITTED	→	OCCUPANCY INDEPENDANCE

ALICE SPD: NEW PILOT CHIP ARCHITECTURE

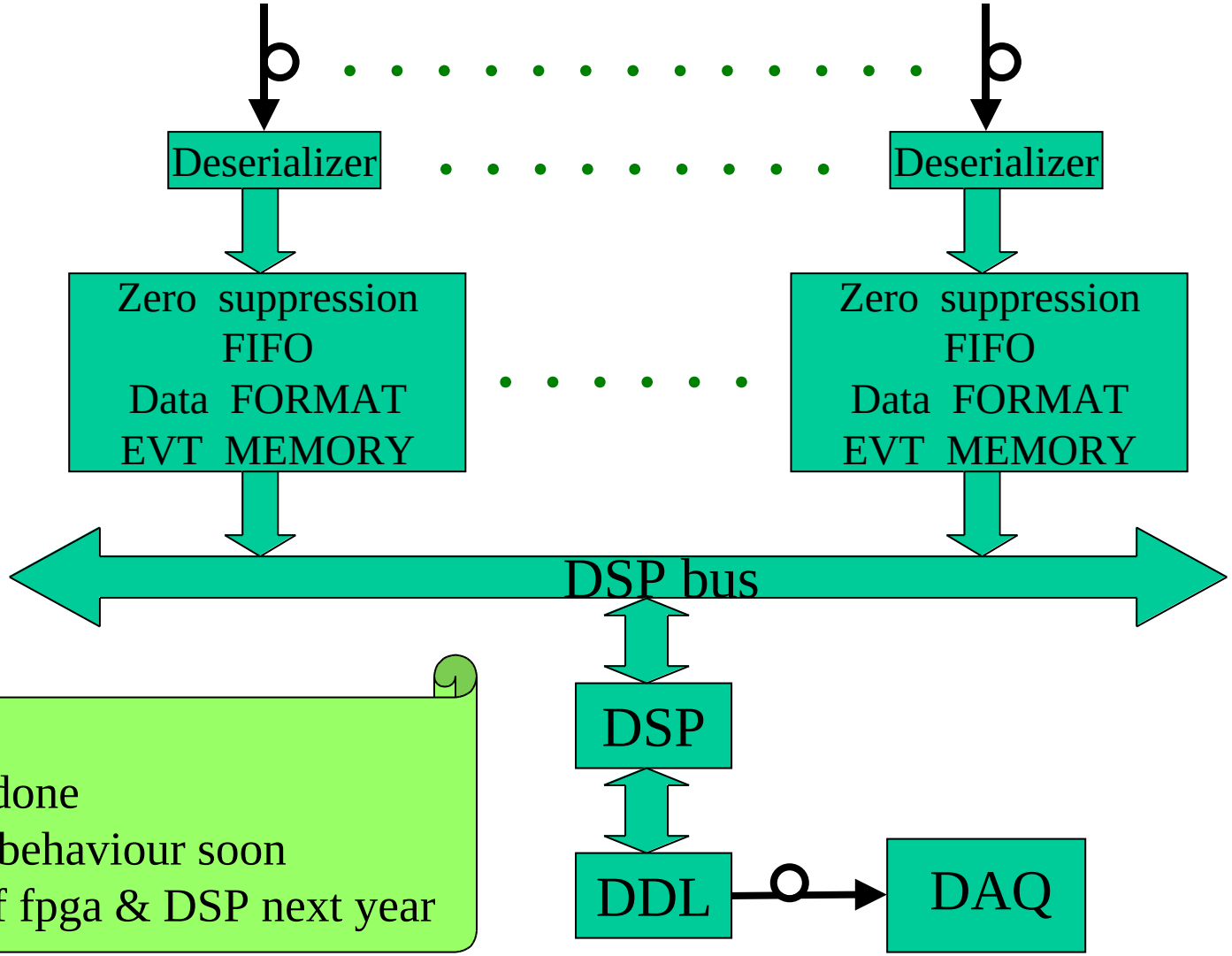


STATUS:

- Chip with serializer & opto-amplifier for the led-laser submitted last year
- Chip with serializer & Glink encoder ready to be submitted this year
- Pixel pilot chip will be submitted by the end of this year
- Chip with Pixel pilot & serializer & opto-amplifier foreseen for next year

ALICE SPD: NEW ROUTER ARCHITECTURE

A VME board version exists now !



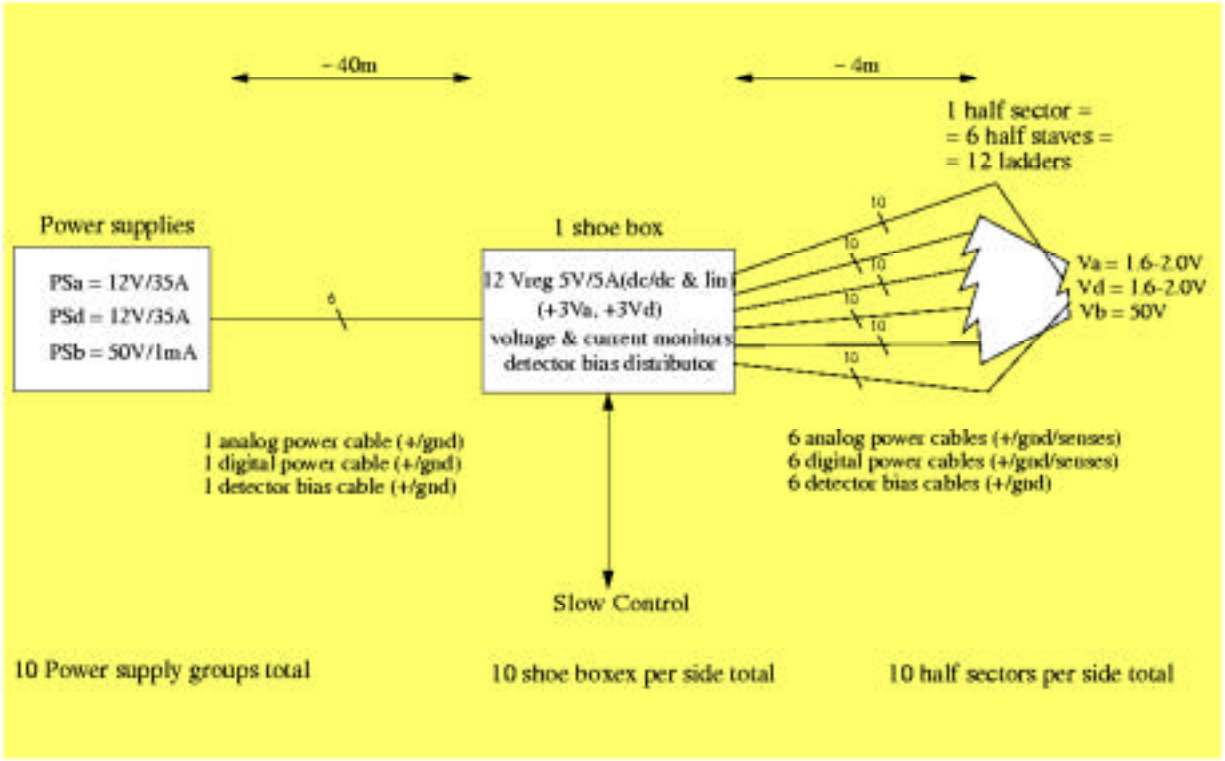
STATUS:

- HDL description done
- Simulation of the behaviour soon
- Implementation of fpga & DSP next year

ALICE SPD: SERVICES ISSUES

Power distribution:

- Power supplies location in “safe area” (~ 40m) outside L3 magnet
- Voltage regulation located on the endcaps (~ 4m) of the TPC? or far (~ 20m) to be faster accessible?
- V & I monitoring done at the level of shoe box

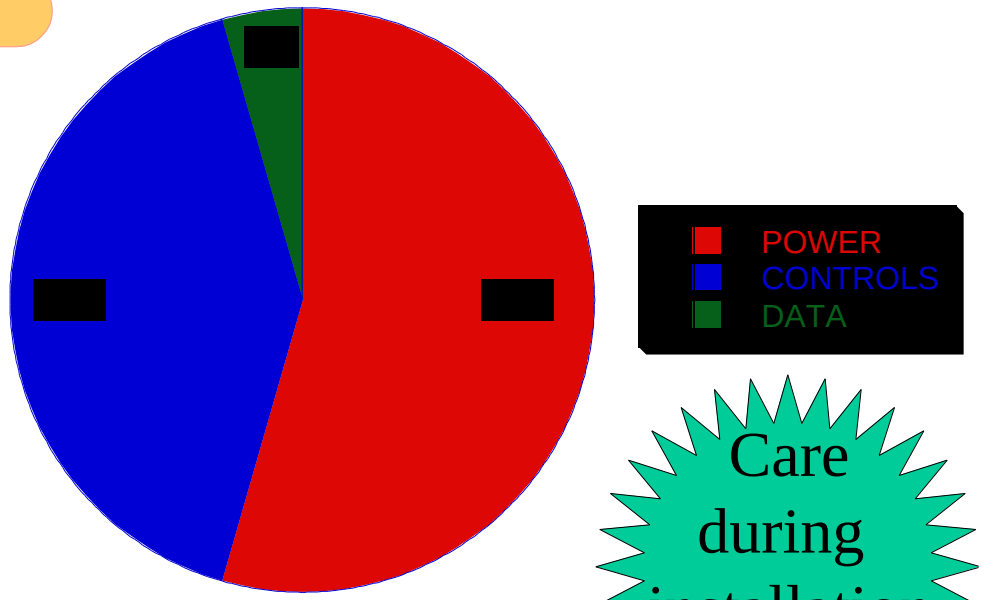


ALICE SPD: FRACTION OF SERVICES WEIGHTS

Cabling between patch panels (endcap) and pixel half-staves

Options:

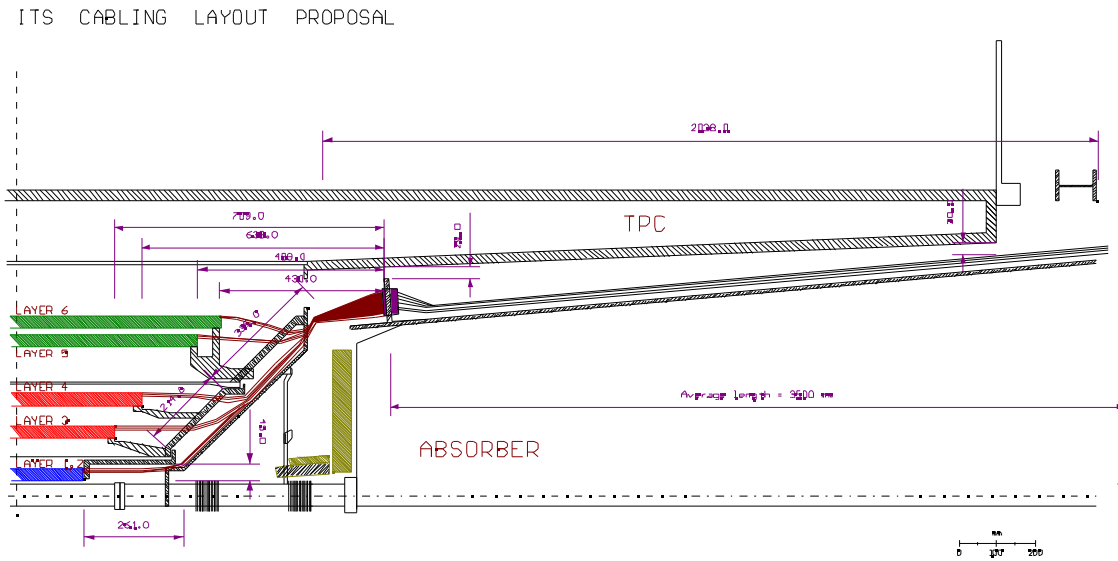
- kapton foil power cables or multiwires ribbon p.c.
- kapton foil signals cables or multiwires ribbon s.c. or multishielded twisted pair s.c.
- optical fiber

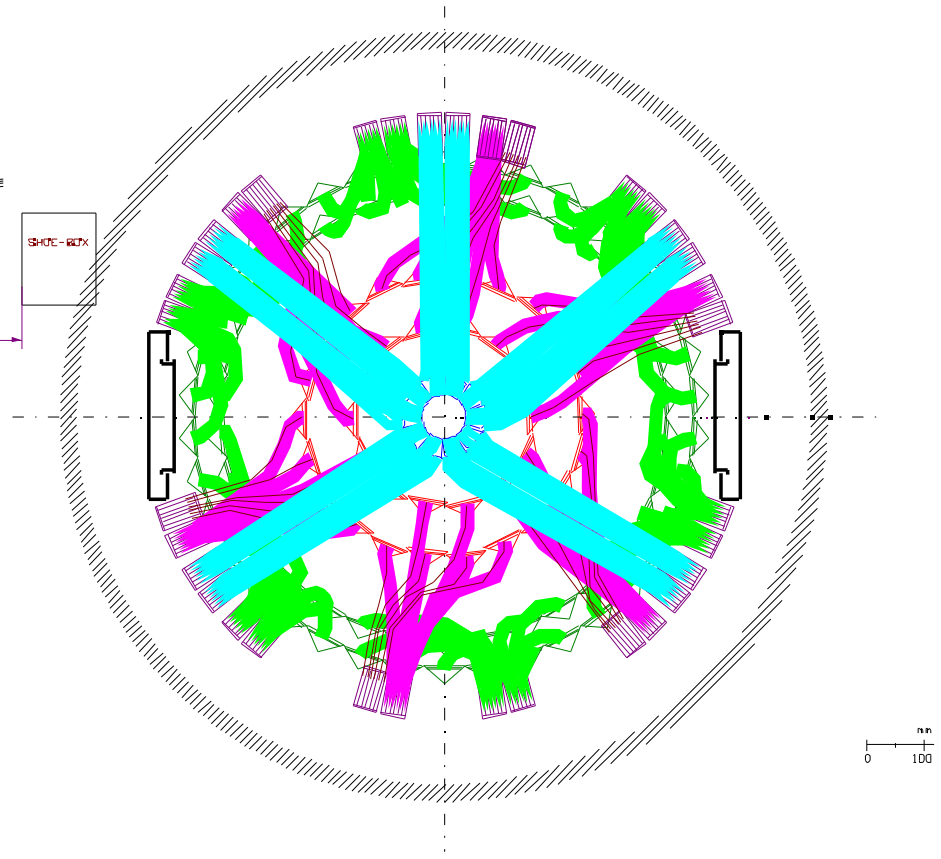


Care during installation !!!

~ 110-140 g/half-stave & ~ 1m long cables system
Total weight for each side ~ 7-8 kg

ALICE SPD: CABLING ISSUE





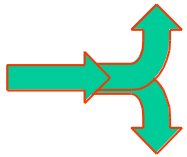
Installation sequence issue:

- SDD+SST
-Beam pipe
- SPD (two half shell)
-TPC

ALICE SPD: CONCLUSIONS

System architecture 

Radiation damage 

Technological aspects 

Infrastructure 

Installation 

ALICE SPD is our QGP gate...