The upgrade of the CMS ECAL Barrel Calorimeter at the HL-LHC

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On behalf of the CMS Collaboration

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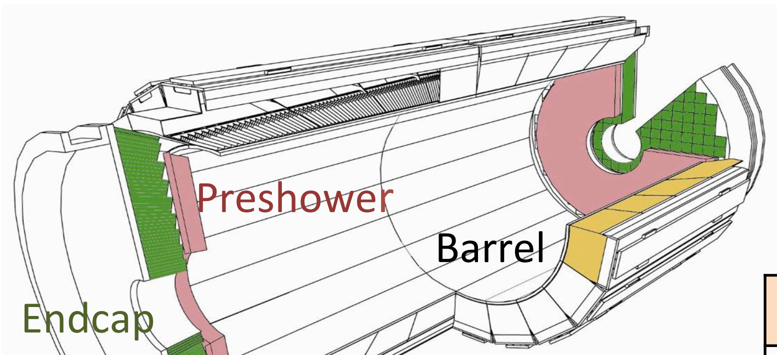
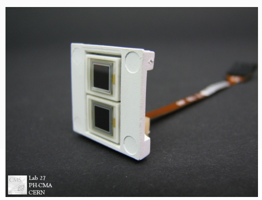
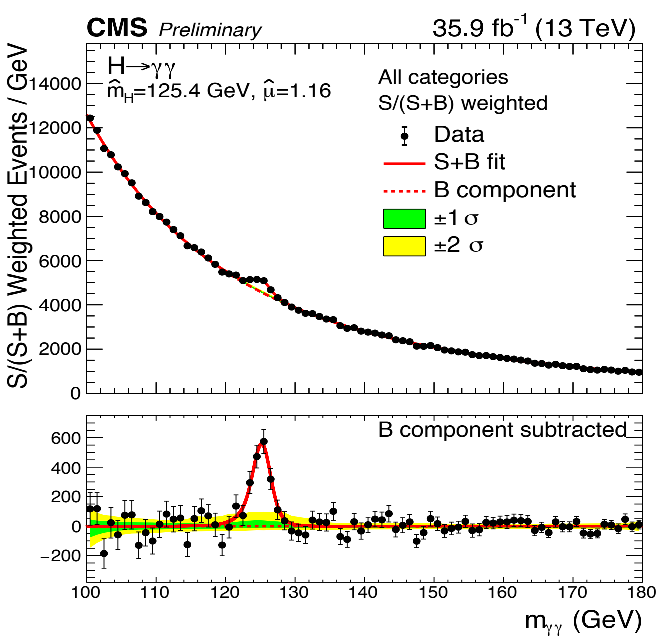
The CMS Electromagnetic Calorimeter





Homogeneous, compact, hermetic
$PbWO_4$ crystals calorimeter
+ Lead/Si Preshower

	coverage	crystals/strips	readout
Barrel (EB)	$\|\eta\|<1.48$	61200	APD
Endcaps (EE)	$1.48<\|\eta\|<3$	14648	VPT
Preshower	$1.65<\|\eta\|<2.6$	137216	



Current design driven by energy performance requirements

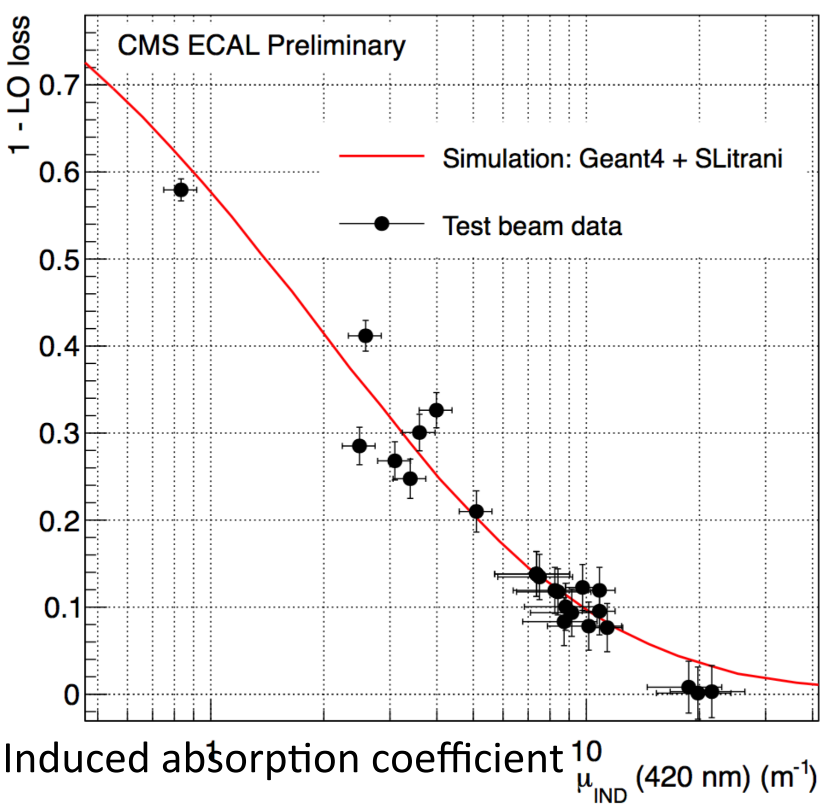
- ECAL crucial for the Higgs boson discovery
- Key component for many searches for new physics and precision measurements

HL-LHC and ECAL crystals

	Inst. Lumi ($cm^{-2}s^{-1}$)	Peak pileup (PU)	Int. Lumi (fb^{-1}/y)	Hadron fluence (particles/cm^2)
LHC	1.7×10^{34}	60	40-50	12×10^{11} (|η|=1), 3×10^{13} (|η|=2.6)
HL-LHC	$5\text{-}7.5 \times 10^{34}$	140-200	250-320	7.6×10^{12} (|η|=1), 2×10^{14} (|η|=2.6)

HL-LHC goal: x10 integrated luminosity

Large increase in pileup and integrated dose wrt LHC



Induced absorption coefficient

Hadron irradiation **of crystals =>**

- **Loss of light output (LO)**
- **Degradation of energy resolution**

Barrel:

- ~50% light after ~3000/fb
- Relatively small energy resolution degradation
- ***Same PbWO+APD technology***

Endcaps *(+ HCAL Endcaps)*

- Will be replaced by HGCAL

EB upgrade: trigger

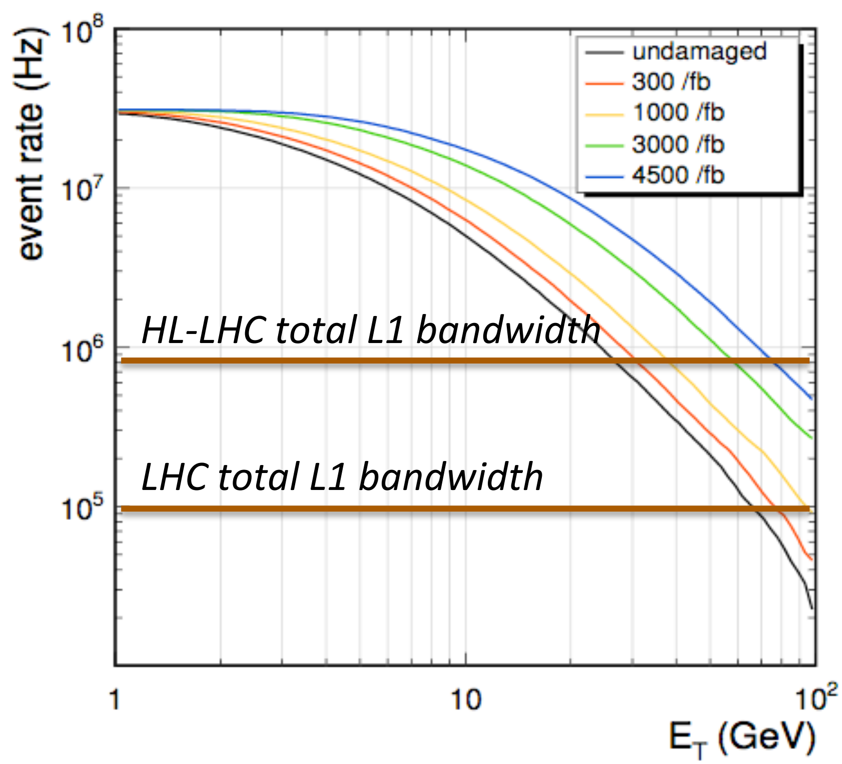
Improved Level-1 trigger (L1) capabilities needed at HL-LHC

- to exploit larger LHC luminosity
- to implement L1 track-trigger

Larger trigger rates and trigger latencies mandatory

- ***Require replacement of ECAL electronics***

ECAL deposits (scintillation + spikes), <PU>=200



Improved rejection of ECAL direct APD signals required

- *"spikes"*, aka large signals due to hadron interactions with the APD
- isolated & faster than scintillation

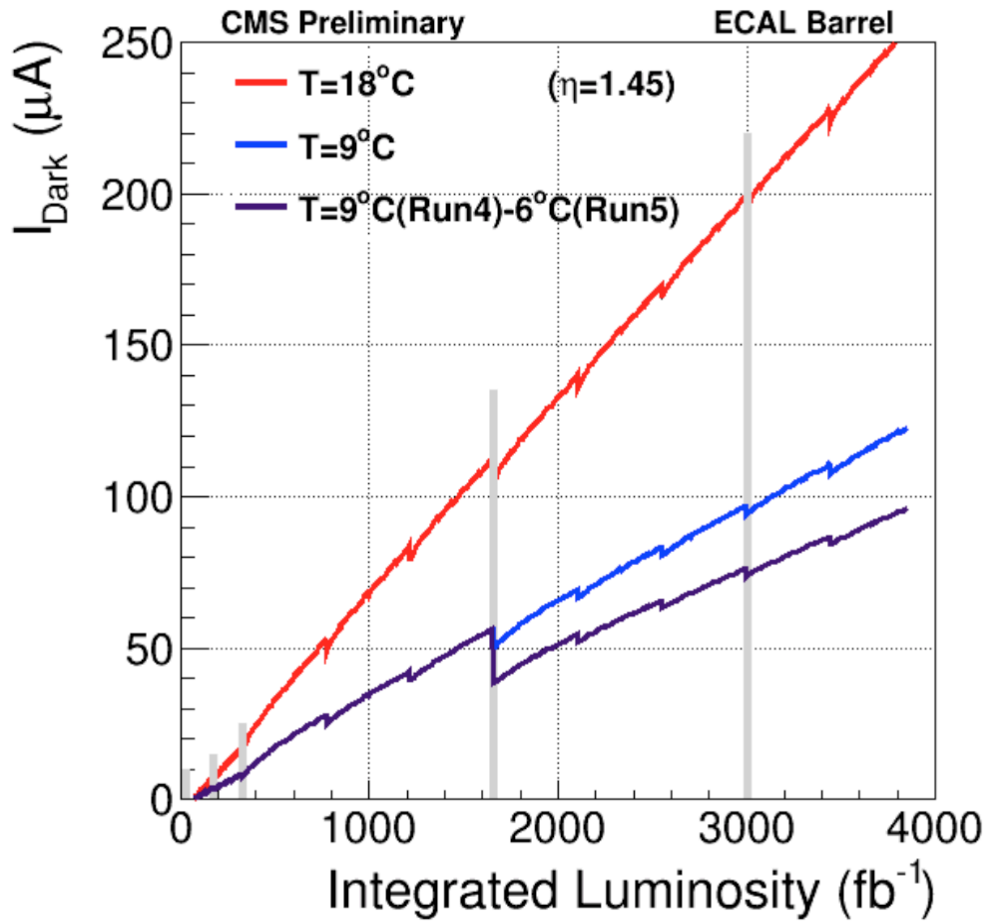
Will dominate L1 rate at HL-LHC otherwise

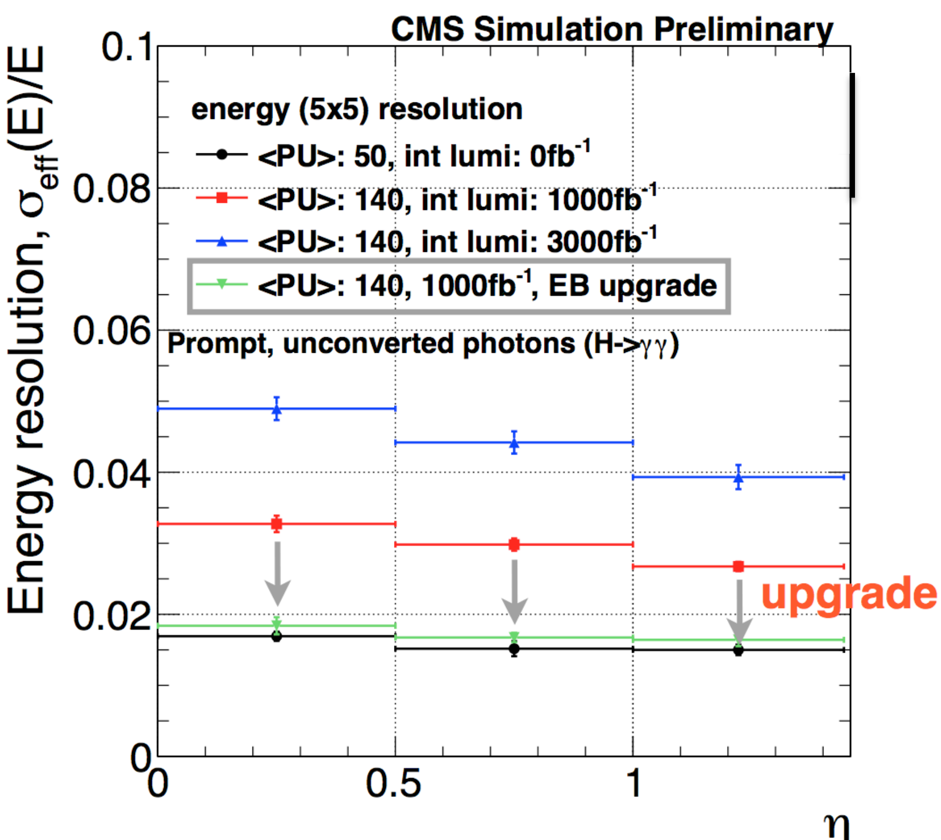
- ***Mitigation needed in new electronics***

APD performance

APDs will experience increased leakage currents due to LHC irradiation

Increase in noise (x10) will significantly degrade the resolution





Mitigation mandatory:

- Barrel cooling: 18°C -> 9°C – 6°C
- New front-end pre-amplifier: shorter pulse shaping

Precision timing

Maintaining reconstruction performance at high (200!!) pileup is a challenge

Eg: H -> γγ

Reduced primary vertex identification efficiency (from recoiling tracks)

- 80% now -> 30% HL-LHC
- **Affects analysis sensitivity**

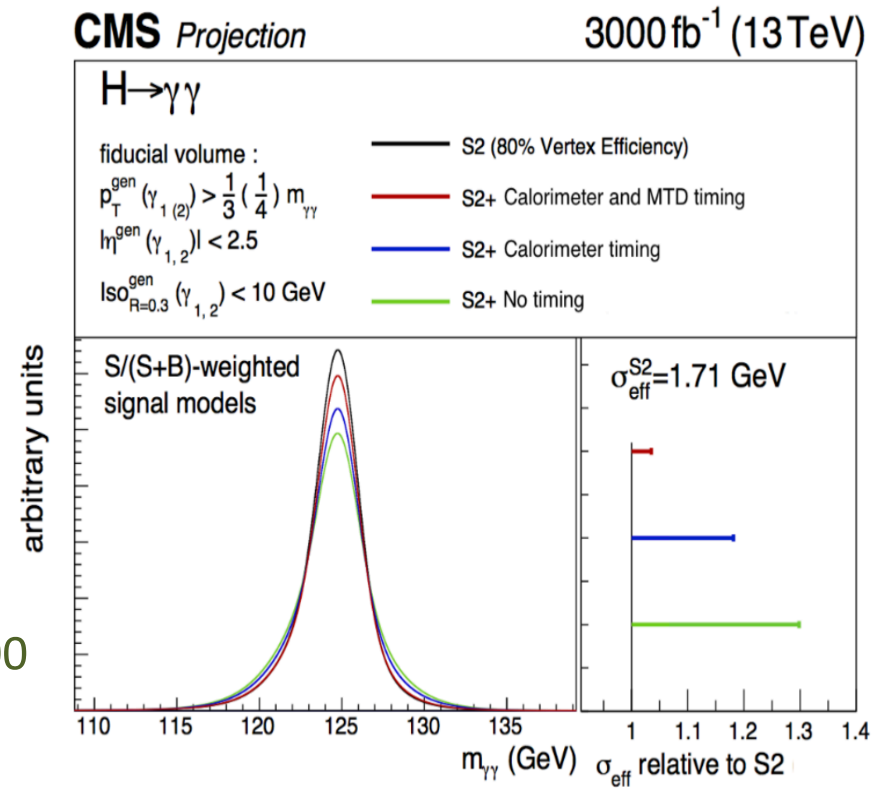
Pileup vertices spread along z *and time*:

Precision timing for charged and neutrals particles key to reduce PU contamination

(See A.Benaglia's talk on CMS dedicated timing detector)

Eg: H -> γγ

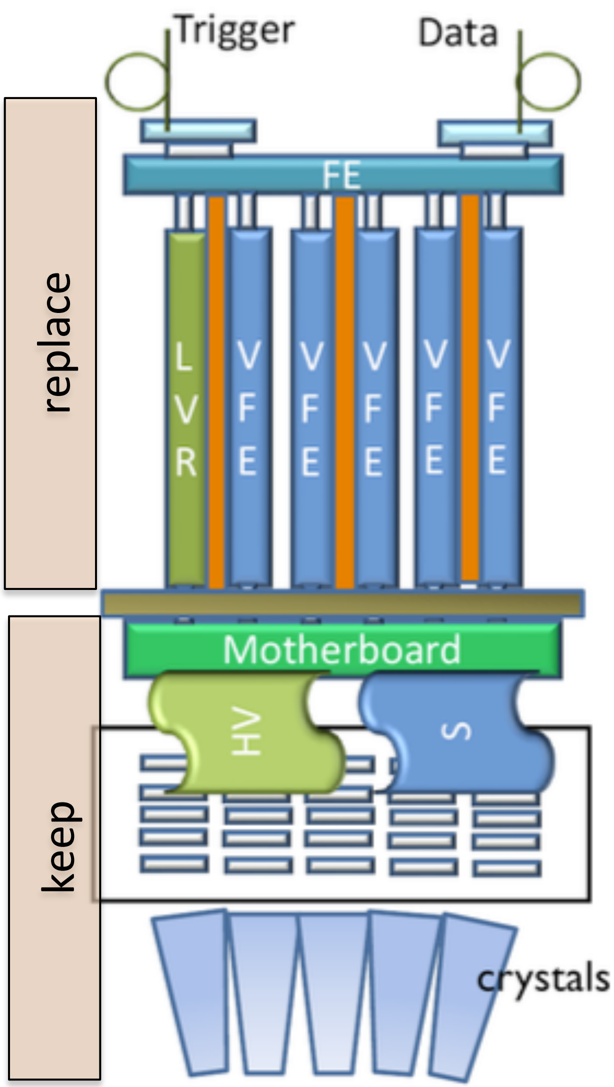
ECAL + track precision timing (30 ps) => ~current vertex localization efficiency at PU=200



Many physics channels can benefit from ECAL precision timing

- Eg: BSM long-lived particles with delayed photons in the final state

EB upgrade highlights



Upgrade needed to maintain excellent performance!

Stay the same: crystals + APDs

New: on-detector electronics (VFE+FE)
- To improve spikes/PU/noise mitigation
- To explore precise (~30ps) time measurement

New: off-detector electronics
- To cope with higher bandwidth from FE

New: operate colder (9°C - 6°C)
- To mitigate APD noise

Replacement of all detector services during CERN LS3
- LV/HV lines, readout and control links
- New cooling system + improved pipes insulation

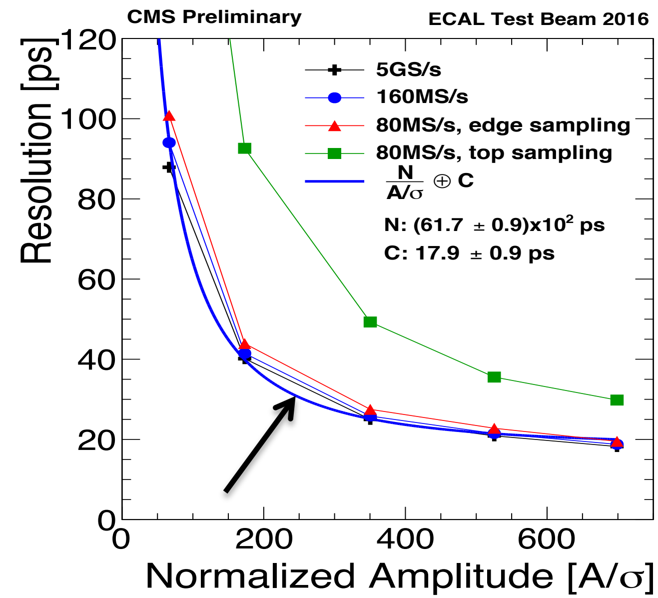
VFE: choice and R&D progress

New VFE boards with re-designed ASICs

- Pre-amplifier:
  Trans Impedance Amplifier (TIA) architecture
    - Two gain ranges (G1, G10), 2 TeV dynamic range
- ADC: custom chip,
  with commercial core and data compression system
    - 12 bit, 160 MHz sampling

Meet physics requirements of HL-LHC optimizing shaping time and sampling rate

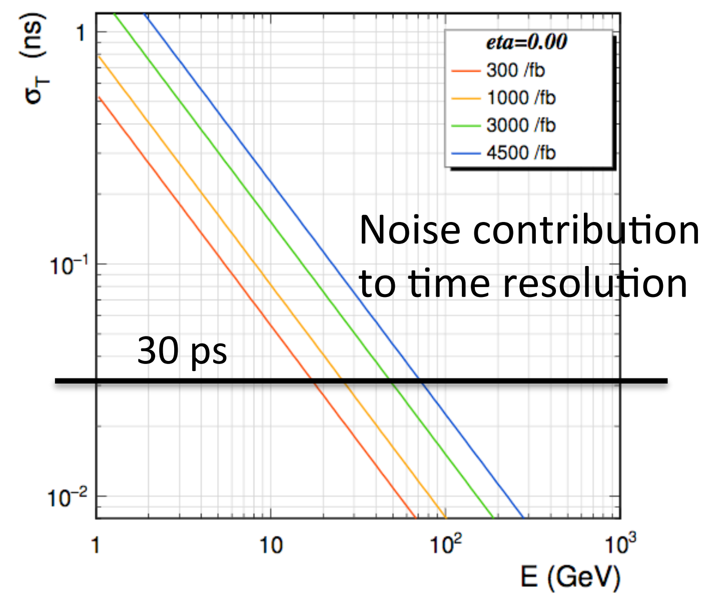
- *noise and PU mitigation, precision timing*



TIA prototype tested in recent test beams

- Noise performance matches expectations
- 30 ps timing resolution achieved at test beam
    - At 25 GeV at HL-LHC start
    - At 60 GeV at HL-LHC end

  With 160 MHz sampling



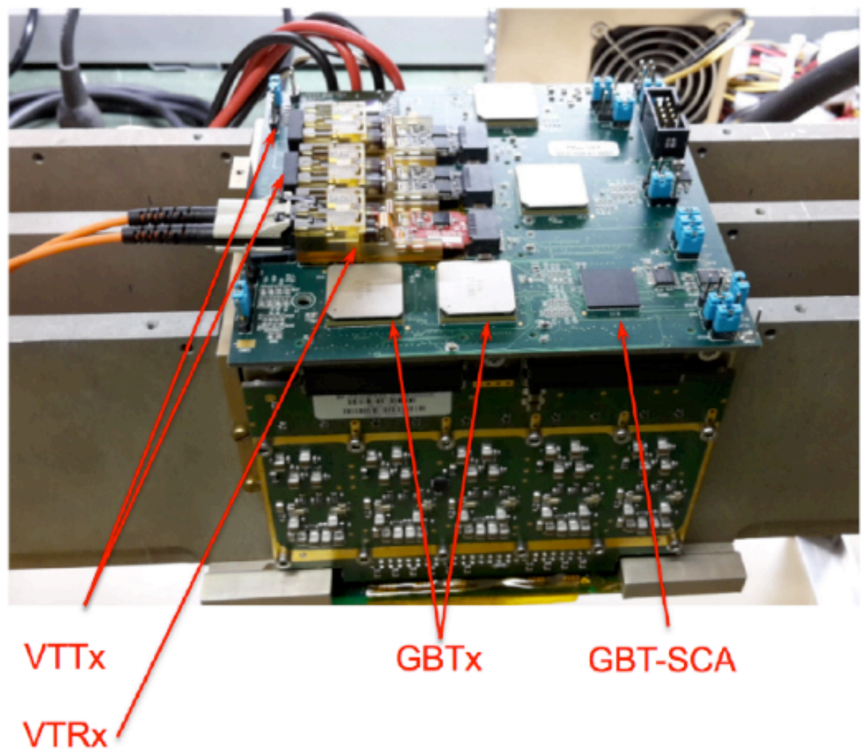
FE: choice and R&D progress

FE cards: transfer all crystal data off-detector
Trigger primitive generation off-detector => no latency buffer/pipeline

High speed optical links: CERN GigaBit Transceiver (GBT) + chipset
- Allows full-granularity readout for trigger
- Data rates: ~30 GB/s per 25 channels with data compression

FE demonstrator
equipped with GBT chips

being tested with legacy VFE and Phase1 trigger boards in CERN testbeams



EB upgrade impact on trigger

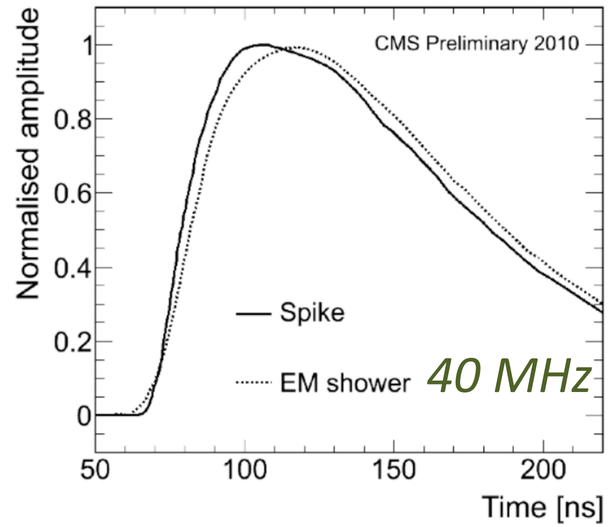
New electronics -> improved information to Level-1 trigger

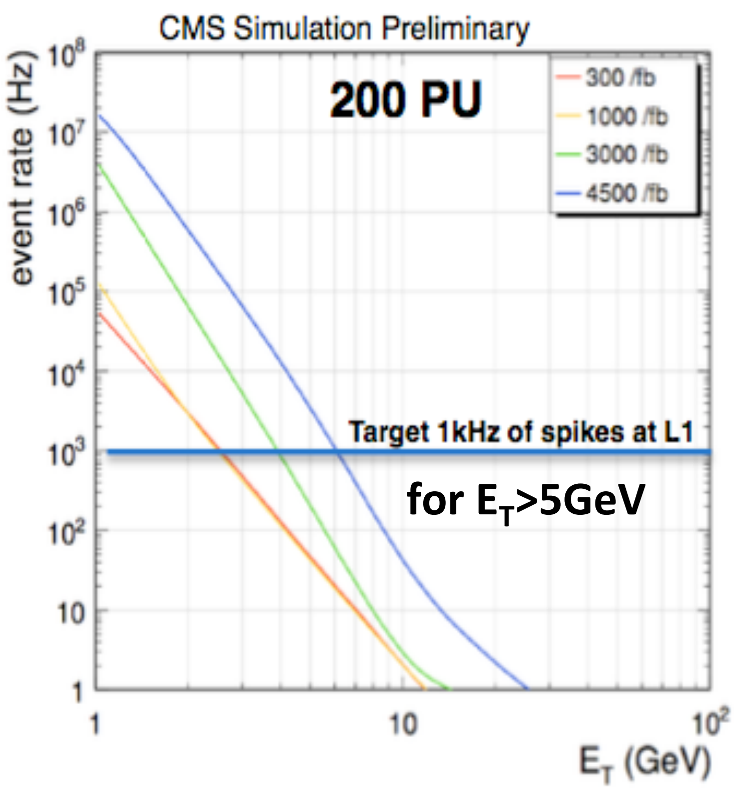
Shorter pulse shaping

- Main handle for spikes discrimination

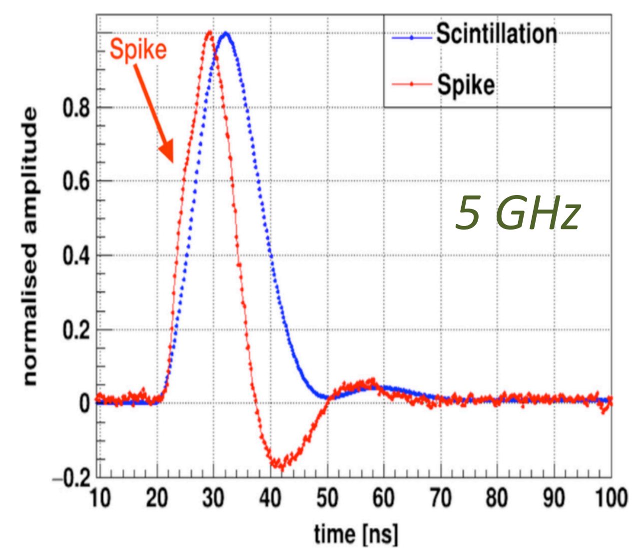
Full granularity at L1 (1x1 crystal, vs current 5x5)

- Advanced clustering algorithms, also matching to L1-tracks
- Event topology as backup for spikes discrimination





Spike-killing algorithm based on pulse shape *performing very well*



Summary

ECAL performance crucial for CMS physics during LHC Run1 and Run2

ECAL barrel upgrade needed to maintain great performance during HL-LHC
- Good noise and pileup mitigation (9°C-6°C)
- Precise time information (30ps)
- Good trigger capabilities (rates, latencies and spikes rejection)

Basic architecture defined and documented in the TDR, published last year
- CERN_LHCC_2017_011; CMS_TDR_015

Prototypes under tests at CERN SPS
ECAL barrel upgrade planned during LHC Long Shutdown 3

Upgraded ECAL barrel detector will still be a key part of CMS during HL-LHC

Backup

Design choices

Pre-amplifier: Trans Impedance Amplifier (TIA) architecture

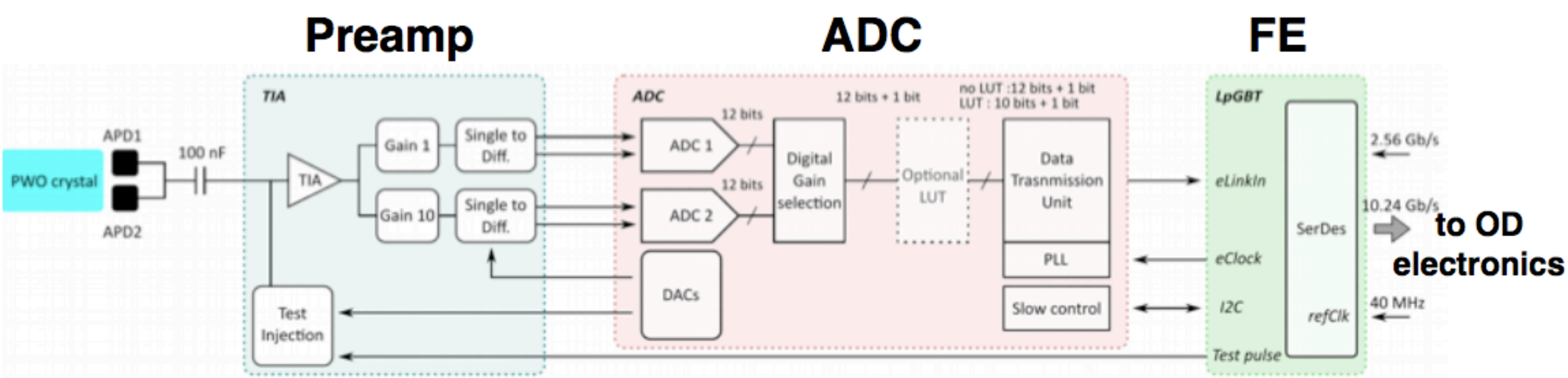
- Two gain ranges (G1, G10). 2 TeV dynamic range, with 50 MeV LSB
- ADC: custom chip, with commercial core and data compression system
- 12 bit, 160 MHz sampling. Dual channel with gain selection logic
- Data transfer unit (DTU) implements data compression before FE

FE: transfer crystal data off-detector using high-speed optical links

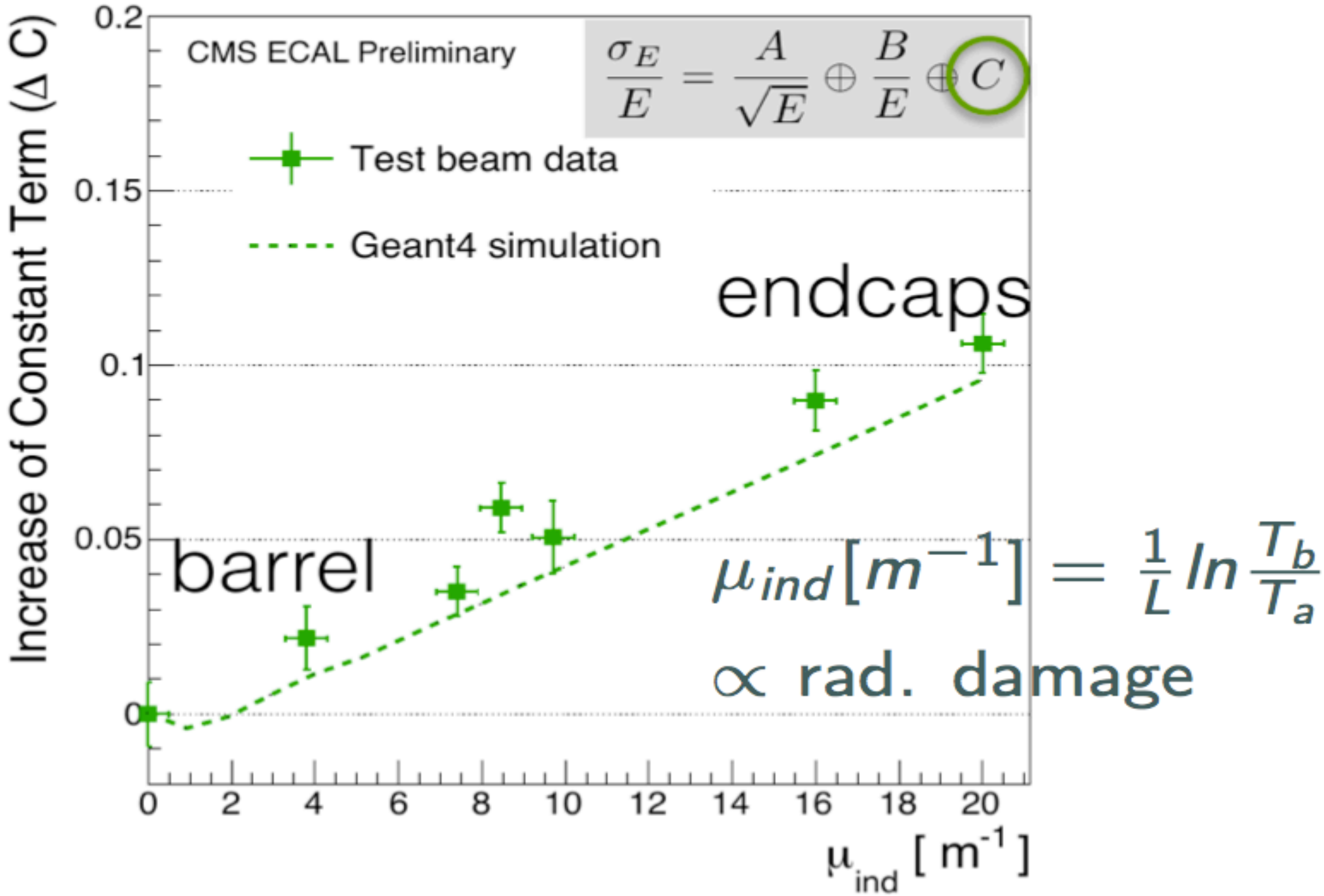
- lpGBT (4x10.24 Gb/s data links, 1x2.56 Gb/s control link)
- eLink serial interface to ADC, clock and slow control

Low voltage regulator (LVR, one every 5x5 crystals)

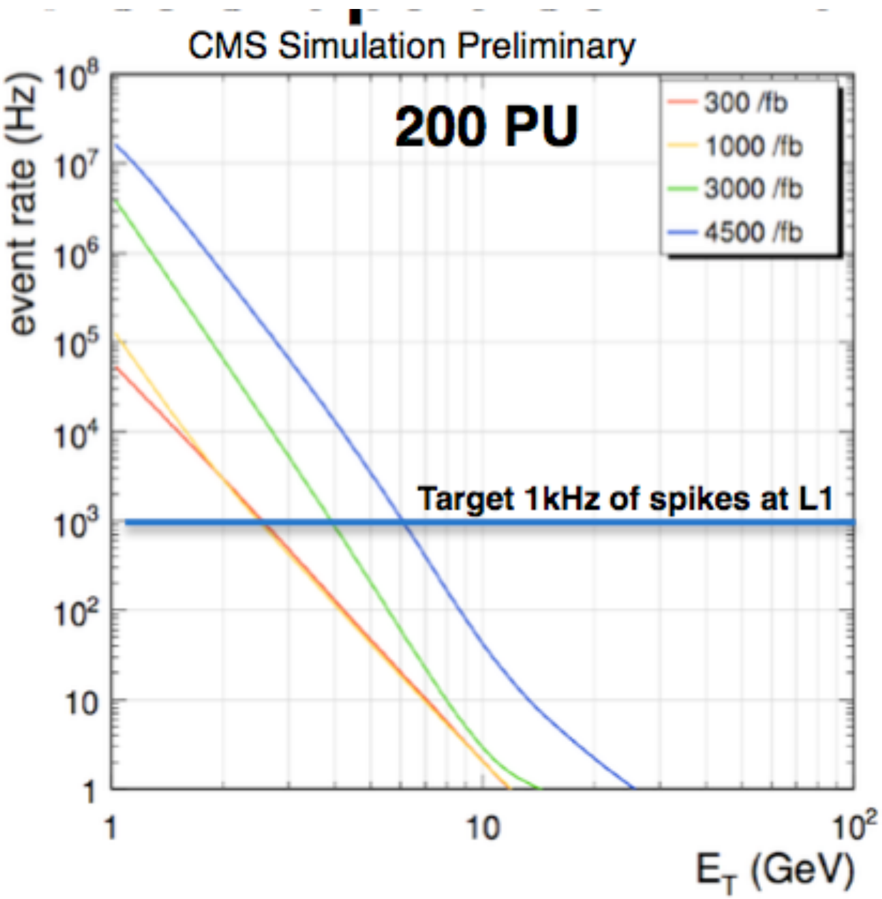
- Needed voltages (1.2V and 2.5V) supplied by point-of-load FEAST DC/DC converters



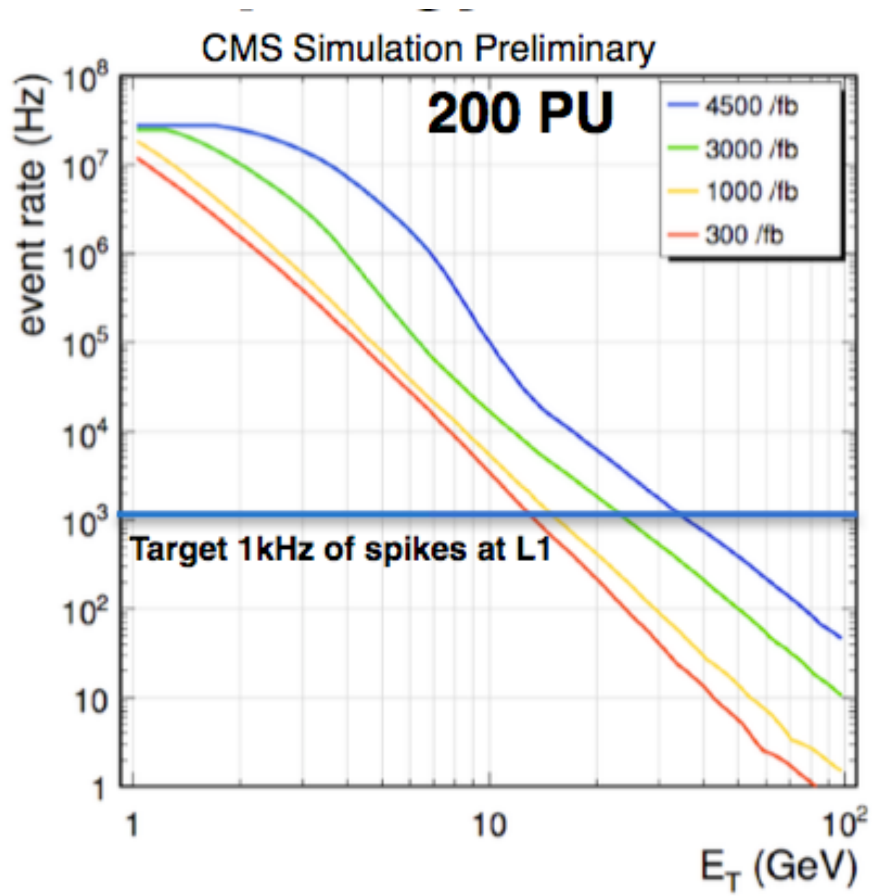
Loss in energy resolution



Spikes rejection



Pulse shape discriminant



Event topology discriminant