Laboratorio di Segnali e Sistemi

Computer /Microprocessori

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Alain Touring (1912-1954)

230 A. M. TURING [Nov. 12,

ON COMPUTABLE NUMBERS, WITH AN APPLICATION TO THE ENTSCHEIDUNGSPROBLEM

By A. M. TURING.

[Received 28 May, 1936.—Read 12 November, 1936.]

The "computable" numbers may be described briefly as the real numbers whose expressions as a decimal are calculable by finite means. Although the subject of this paper is ostensibly the computable *numbers*, it is almost equally easy to define and investigate computable functions of an integral variable or a real or computable variable, computable predicates, and so forth. The fundamental problems involved are, however, the same in each case, and I have chosen the computable numbers for explicit treatment as involving the least cumbrous technique. I hope shortly to give an account of the relations of the computable numbers, functions, and so forth to one another. This will include a development of the theory of functions of a real variable expressed in terms of computable numbers. According to my definition, a number is computable if its decimal can be written down by a machine.

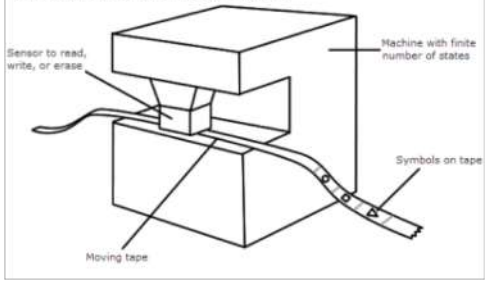
In §§ 9, 10 I give some arguments with the intention of showing that the computable numbers include all numbers which could naturally be regarded as computable. In particular, I show that certain large classes of numbers are computable. They include, for instance, the real parts of all algebraic numbers, the real parts of the zeros of the Bessel functions, the numbers π, e, etc. The computable numbers do not, however, include all definable numbers, and an example is given of a definable number which is not computable.

Although the class of computable numbers is so great, and in many ways similar to the class of real numbers, it is nevertheless enumerable. In § 8 I examine certain arguments which would seem to prove the contrary. By the correct application of one of these arguments, conclusions are reached which are superficially similar to those of Gödel†. These results

† Gödel, "Über formal unentscheidbare Sätze der Principia Mathematica und verwandter Systeme, I", *Monatshefte Math. Phys.*, 38 (1931), 173–198.

A wartime picture of a Bletchley Park Bombe

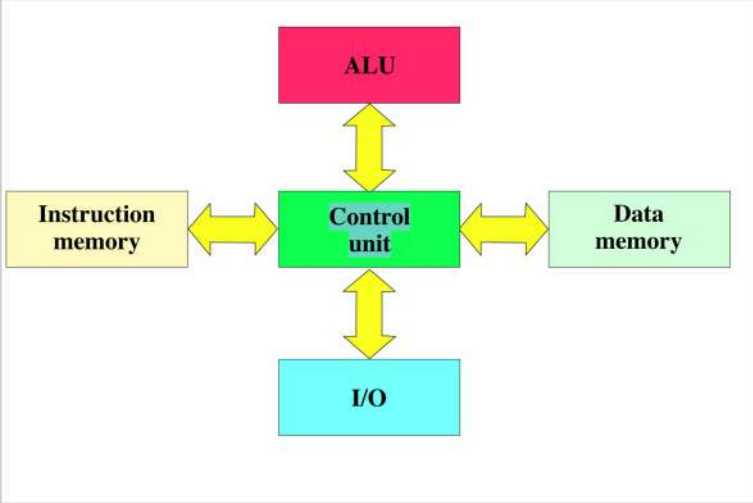
A Turing machine is a theoretical generalized computer, composed of a tape on which symbols representing instructions are imprinted. The tape can move backwards and forwards in the machine, which can read the intructions and write the resultant output back onto the tape.

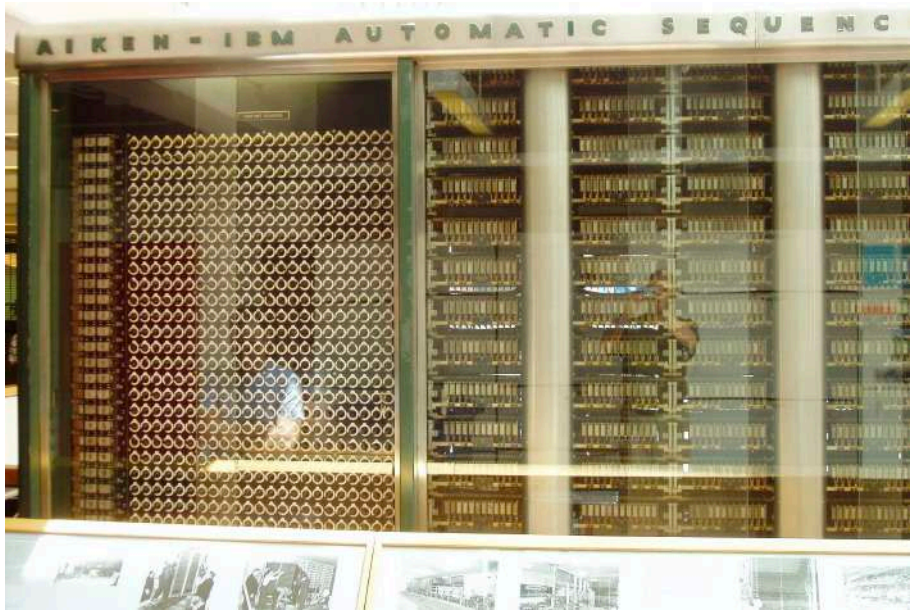


Enigma Machine

The bombe is an electro-mechanical device used by British cryptologists to help decipher German Enigma-machine-encrypted secret messages during World War II.[1] The US Navy[2] and US Army[3] later produced their own machines to the same functional specification, albeit engineered differently both from each other and from the British Bombe itself.

Harvard Architecture (1937)



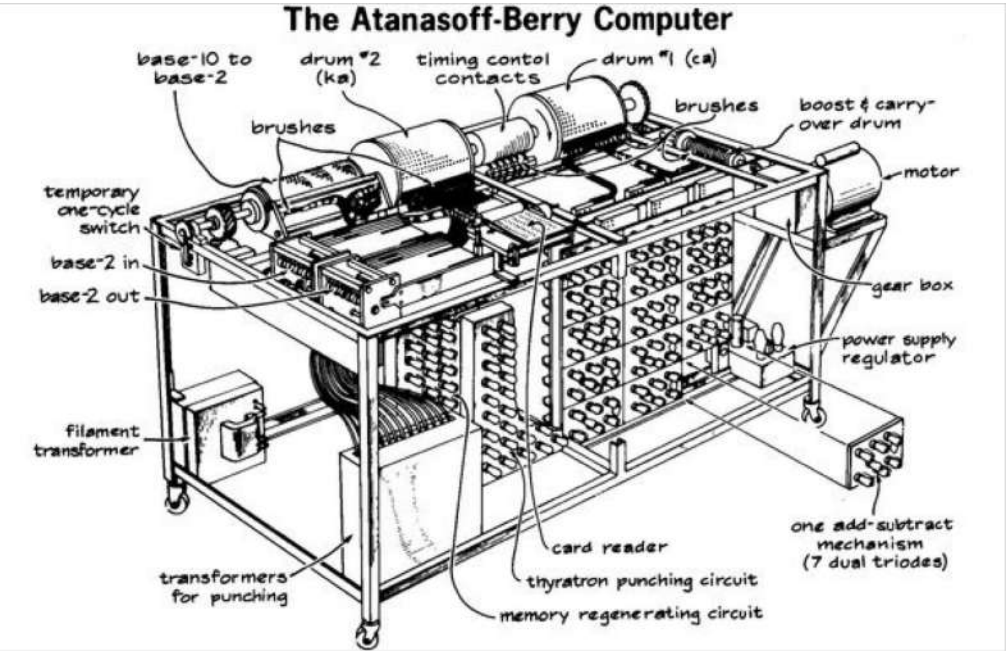


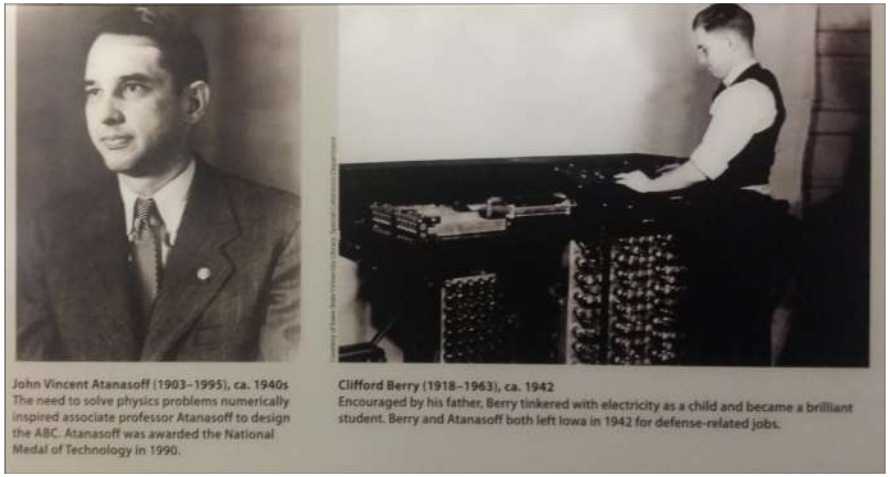
Howard Hathaway Aiken (March 8, 1900 – March 14, 1973) was an American physicist and a pioneer in computing, being the original conceptual designer behind IBM's Harvard Mark I computer.[2]

Mark I by Harvard University's staff,[1] was a general purpose electromechanical computer that was used in the war effort during the last part of World War II.

One of the first programs to run on the Mark I was initiated on 29 March 1944[2] by John von Neumann. At that time, von Neumann was working on the Manhattan project, and needed to determine whether implosion was a viable choice to detonate the atomic bomb that would be used a year later.

ABC Computer (Primo computer digitale 1937)





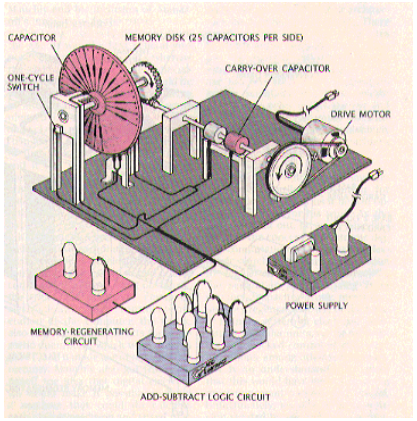
Dipartimento di Fisica dell'Iowa State University.
Il prototipo fu realizzato nel novembre del 1939.

- Risoluzione Equazioni lineari (29 variabili)
- 320 chilogrammi
- 1.6 chilometri di cavi,
- 280 valvole termoioniche,
- 31 thyratron
- Sistema binario
- Utilizzo di memorie a condensatore con circuito di refresh

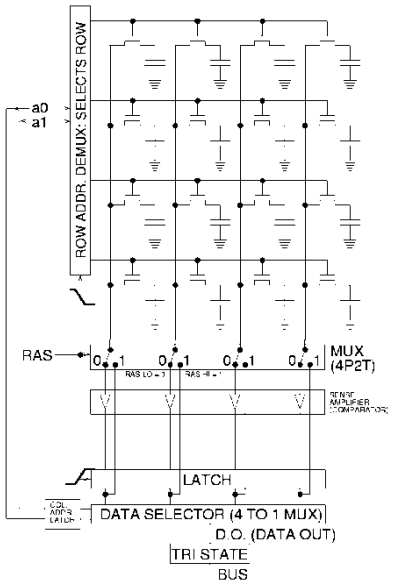
Computer History Museum

Memorie digitali

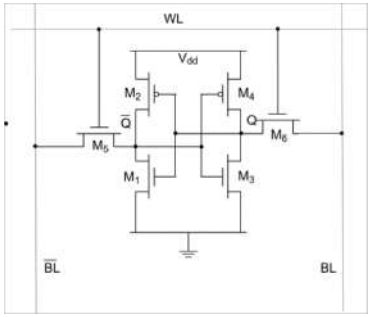
Memorie Dinamiche

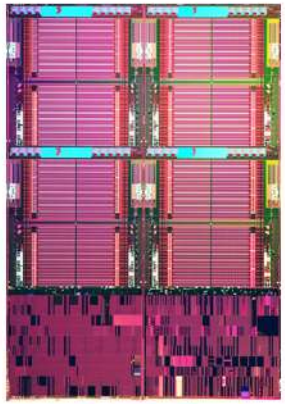


http://it.wikipedia.org/wiki/Atanasoff-Berry_Computer



Memorie Statiche



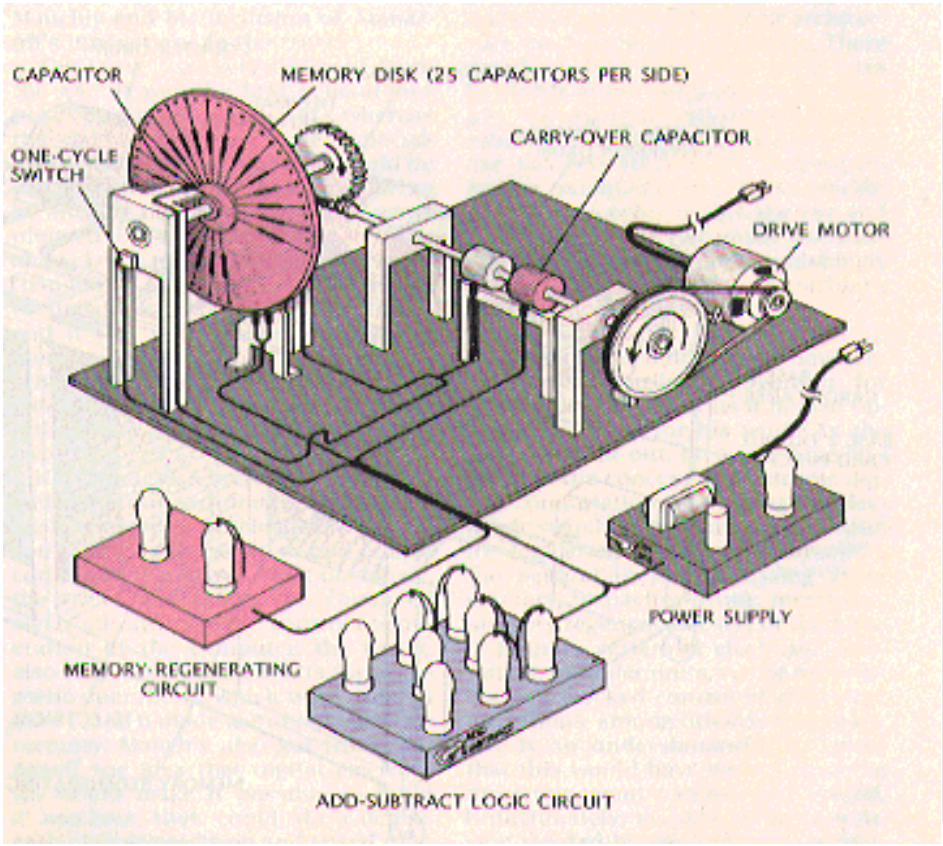


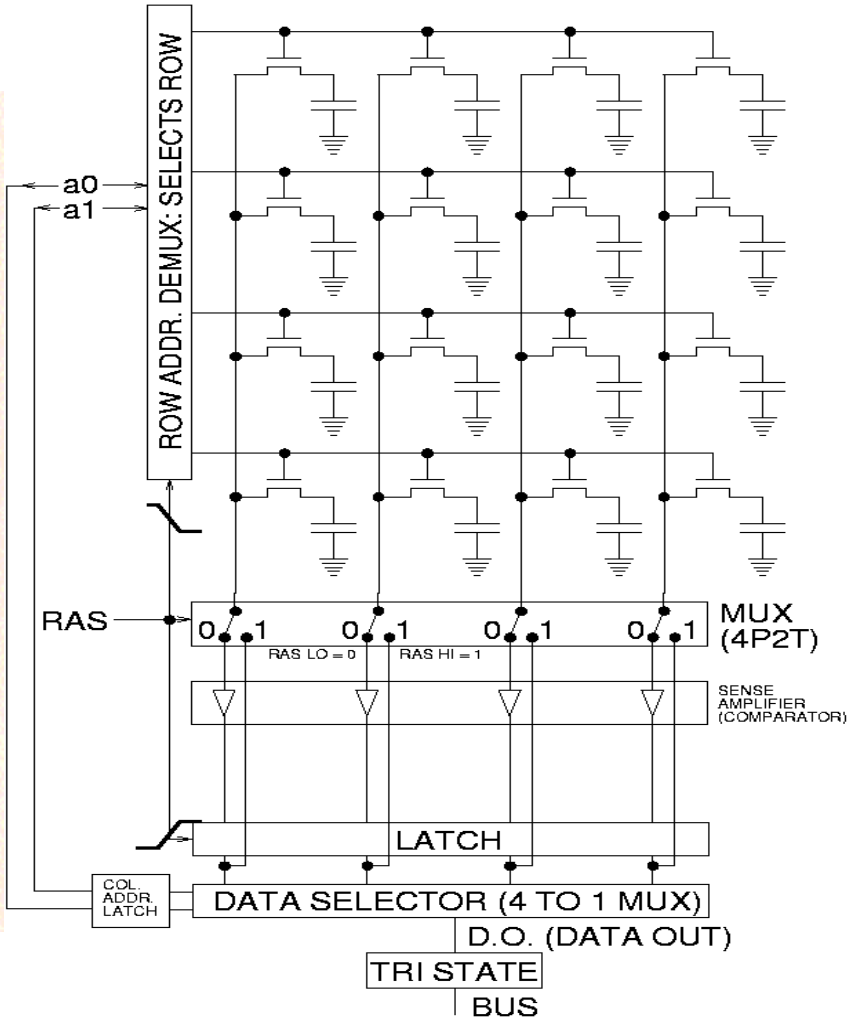
http://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/05-switched/40-cmos/sramcell.html

Semiconductor manufacturing processes

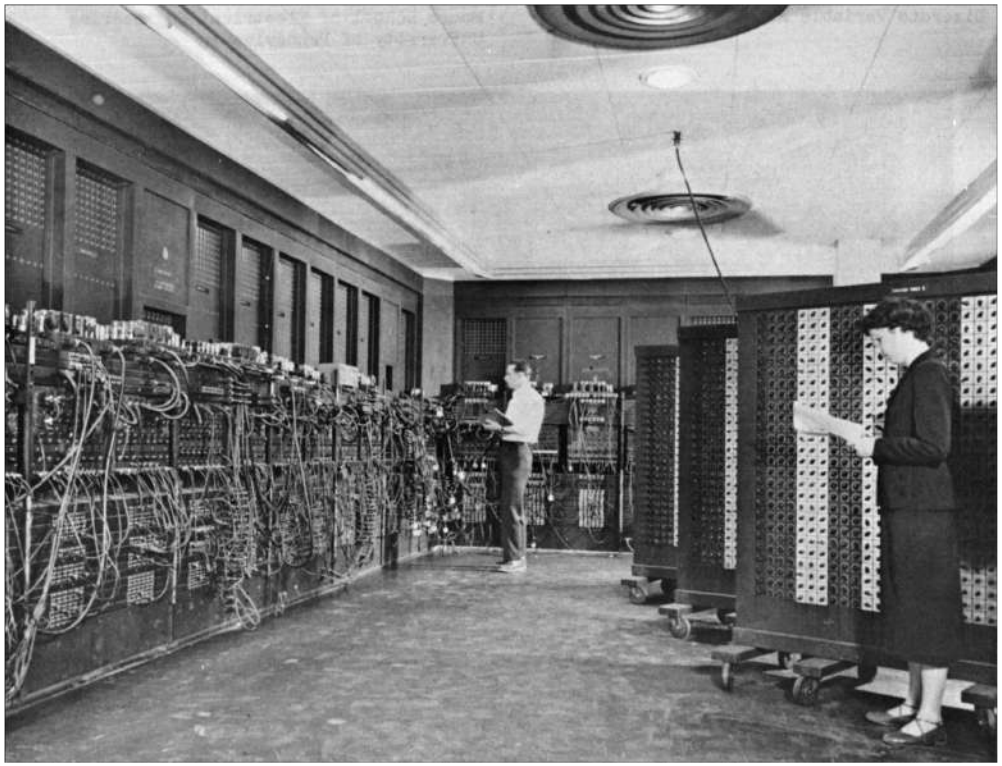
- 10 µm — 1971
- 3 µm — 1975
- 1.5 µm — 1982
- 1 µm — 1985
- 800 nm (.80 µm) — 1989
- 600 nm (.60 µm) — 1994
- 350 nm (.35 µm) — 1995
- 250 nm (.25 µm) — 1998
- 180 nm (.18 µm) — 1999
- 130 nm (.13 µm) — 2000
- 90 nm — 2002
- 65 nm — 2006
- 45 nm — 2008
- **32 nm** — 2010
- 22 nm — 2011
- 16 nm — approx. 2013
- 11 nm — approx. 2015
- 6 nm — approx. 2020
- 4 nm — approx. 2022

Memorie dinamiche





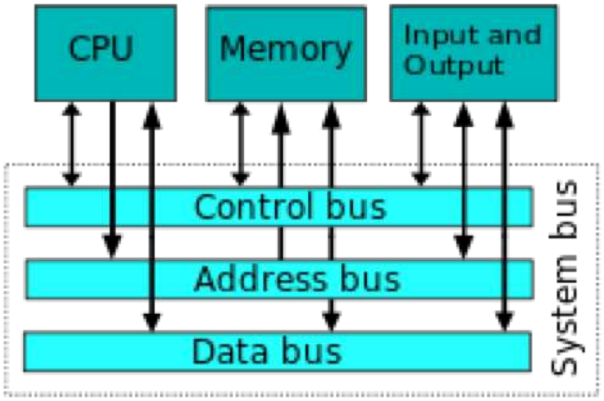
ENIAC (1946)

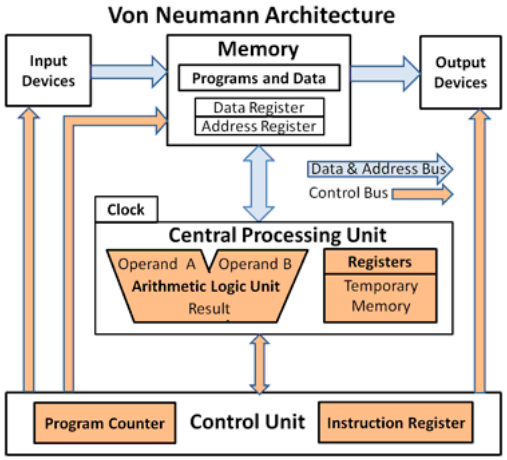


John Presper Eckert
(1919-1995)
and
John Mauchly
(1907-1980)
of the
University of Pennsylvania Moore School of Engineering

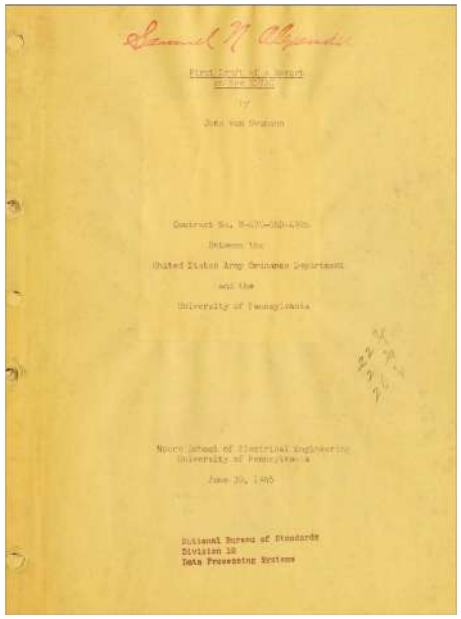
- 18.000 valvole termoioniche,
- 500.000 contatti saldati manualmente, 1.500 relè
- potenza termica di circa 200 kW

Von Neumann architecture (1945)



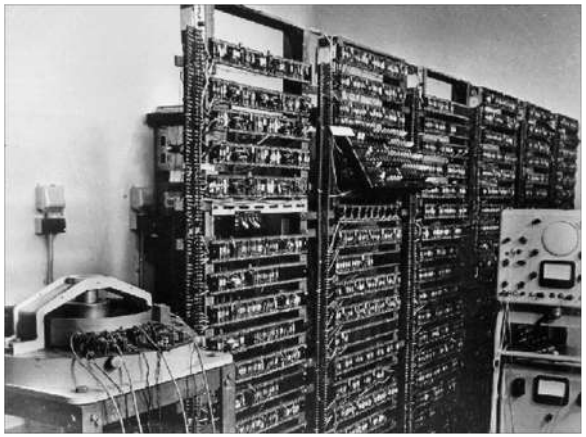


John von Neumann (1903 – 1957) mathematician, physicist,computer scientist, and polymath. He made major contributions to a number of fields, including mathematics (foundations of mathematics, functional analysis, ergodic theory, representation theory, operator algebras, geometry, topology, and numerical analysis), physics (quantum mechanics, hydrodynamics, and quantum statistical mechanics), economics (game theory), computing (Von Neumann architecture, linear programming, self-replicating machines, stochastic computing), and statistics.

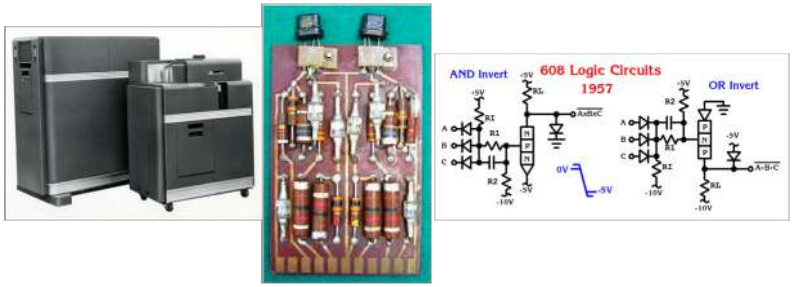


First Draft of a Report on the EDVAC is an incomplete 101-page document written by John von Neumann and distributed on June 30, 1945 by Herman Goldstine

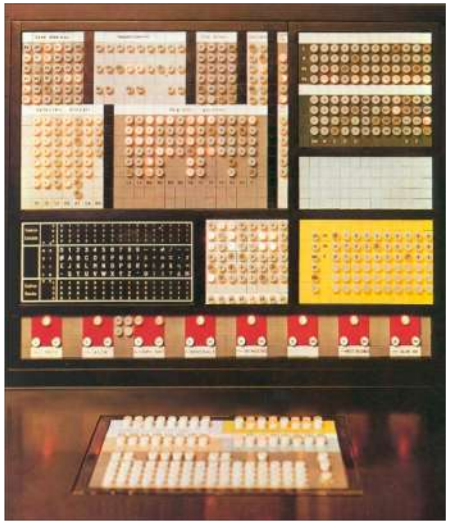
Seconda generazione Computer a Transistor



The University of Manchester's experimental Transistor Computer was first operational in November 1953 and it is widely believed to be the first transistor computer to come into operation anywhere in the world. Wikipedia



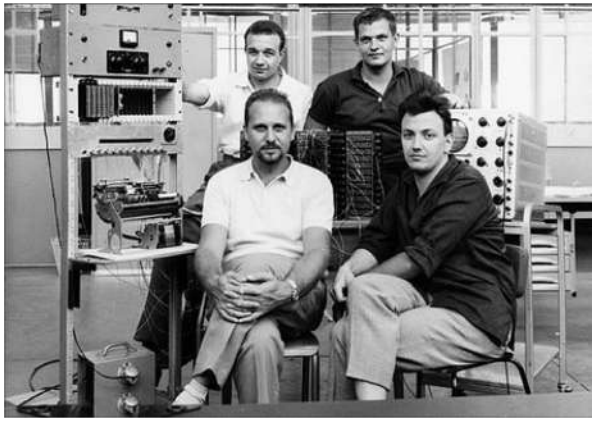
The **IBM 608 Transistor Calculator**, a plugboard-programmable unit, was the first IBM product to use transistor circuits without any vacuum tubes and is believed to be the world's first all-transistorized calculator to be manufactured for the commercial market.[1][2]:34 Announced in April 1955,[3][4] it was released in December 1957. The 608 was withdrawn from marketing in April 1959.[3] Wikipedia



olivetti elea 9003

Elea 9003 (Macchina 1T - Machine 1T), prototype in 1958, announced in 1959,[2][1]:41,47 designed entirely in discrete (diode–transistor logic), was the first fully transistorized commercial computer.[With industrial design by Ettore Sottsass, it was leased to about 40 individual customers, of which the first (Elea 9003/01) was installed at the textile company Marzotto[4] and second (Elea 9003/02) to Monte dei Paschi di Siena.[5] Later this unit was donated for educational purposes. Other mainframes were leased to insurance companies and energy companies. Wikipedia

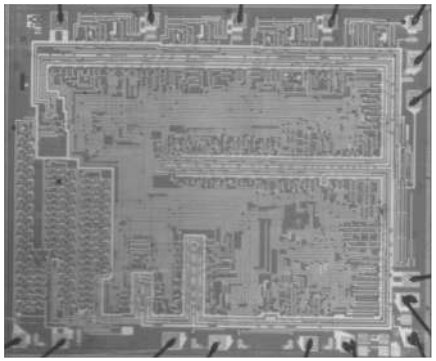
Olivetti P101 il primo personal ?

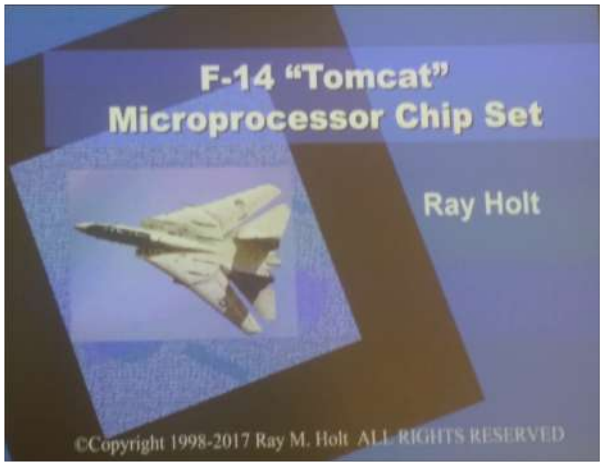


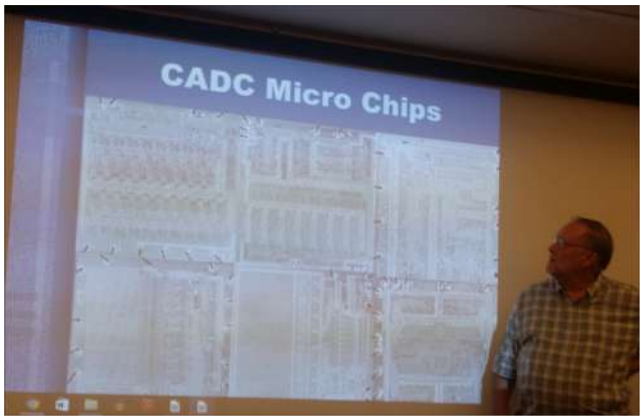
L'**Olivetti Programma 101** (in acronimo **P101**) è stato un computer sviluppato dalla ditta italiana Olivetti negli anni tra il 1962 e il 1964 e prodotto tra il 1965 e il 1971. Presentato per la prima volta alla grande esposizione dei prodotti per ufficio BEMA di New York nell'ottobre 1965, fu progettato dall'ingegnere Pier Giorgio Perotto[4] (in omaggio al quale assunse il soprannome di **Perottina**) insieme a Giovanni De Sandre e Gastone Garziera.[5] Il designer Mario Bellini le conferì un disegno avveniristico per l'epoca.

È considerato il primo "computer da scrivania" commerciale programmabile motivo per cui vieni definito anche come il **primo Personal Computer** della storia.[6][7][8]

The First Microprocessor Ray Holt (1971)







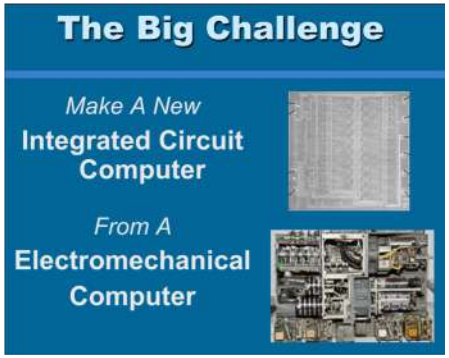
INTRODUCTION

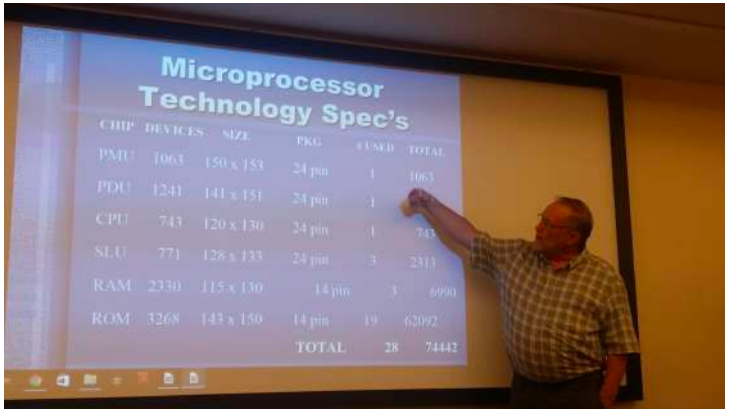
This paper describes the architecture of the CPU and Memory for the Central Air Data Computer (CADC) System used in the Grumman/Navy F14A carrier-based fighter aircraft. The CADC performs specialized computerational functions in response to input stimuli such as pressure sensors, temperature sensors and closed loop feedback inputs. Outputs from the CADC system are used to drive pilot visual displays (such as, altimeter, temperature indicator, mach number indicator, etc.) and to provide control inputs for other aircraft systems. The outputs from the CADC are in the form of digital and analog signals. Figure 1 illustrates a block diagram for the CADC.

Being in a flight environment meant that certain constraints must greatly reflect the architecture of the CPU and Memory. These constraints were size, power, real-time computing capability and cost, not necessarily in that order. Other constraints such as temperature, acceleration and mechanical shock affected the overall design of the CADC.

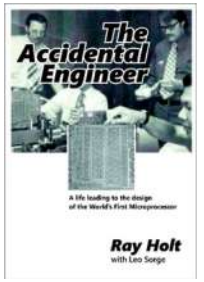
The size of the CPU-Memory was limited to a maximum of 40 square inches. This included the arithmetic section, read-only memory, and read/write memory. Since the unit was to be packaged on a printed circuit card the number of layers of the p.c. card was an important consideration. The power consumption had a limit of 10 watts at ambient 25°C. This was principally a function of the capabilities of the p.c. card to withstand the heat.

The required computing capacity for the CPU was not defined at the beginning. This meant that the system had to be somewhat flexible to changes in computational load. Of course limits had to be set to be able to work within the other constraints. What was known about the computation was the form of the equations to be implemented. This included polynominal evaluations, data limit-

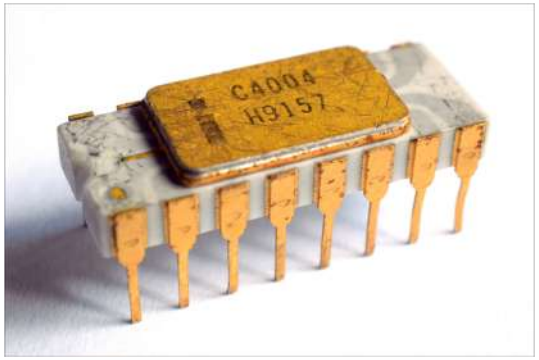




In 1968, Garrett AiResearch (who employed designers Ray Holt and Steve Geller) was invited to produce a digital computer to compete with electromechanical systems then under development for the main flight control computer in the US Navy's new F-14 Tomcat fighter. The design was complete by 1970, and used a MOS-based chipset as the core CPU. The design was significantly (approximately 20 times) smaller and much more reliable than the mechanical systems it competed against, and was used in all of the early Tomcat models. This system contained "a 20-bit, pipelined, parallel multi-microprocessor". The Navy refused to allow publication of the design until 1997. For this reason the CADC, and the MP944 chipset it used, are fairly unknown.Ray Holt's autobiographical story of this design and development is presented in the book: The Accidental Engineer.[15][16]

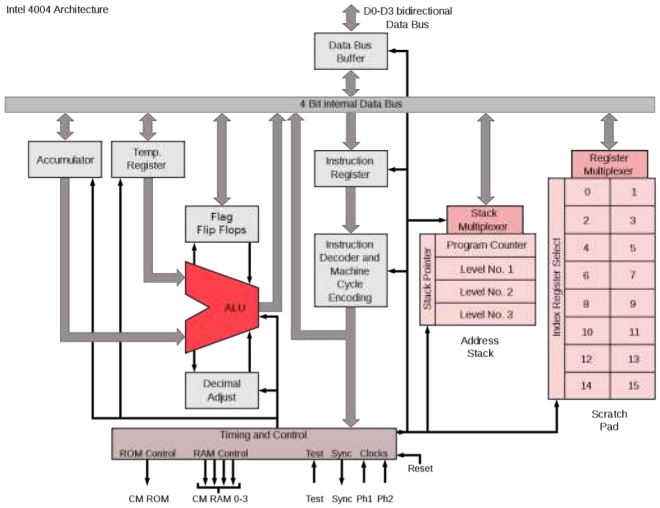


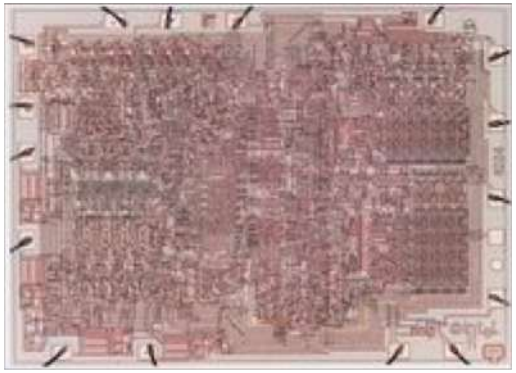
The First commercial microprocessor



The chip design started in April 1970, when Federico Faggin joined Intel, and was completed under his leadership in January 1971. The first commercial sale of the fully operational 4004 occurred in March 1971 to Busicom Corp.

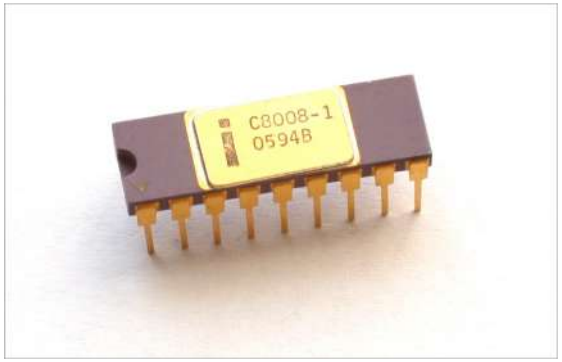
Intel 4004





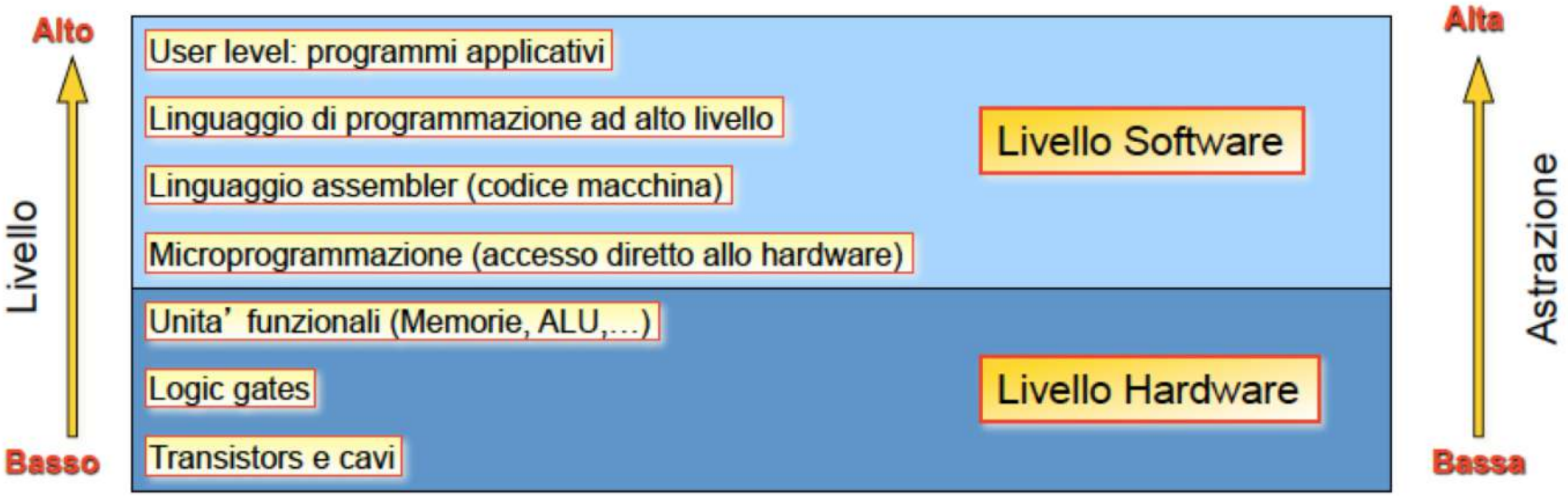
.**Federico Faggin** (Vicenza, 1º dicembre 1941)
èun fisico, inventore e imprenditore italiano naturalizzato statunitense[1].
Dal 1968 Faggin risiede negli Stati Uniti ed ha assunto anche la cittadinanza statunitense. Fu capo progetto dell'Intel 4004 e responsabile dello sviluppo dei microprocessori 8008, 4040 e 8080 e delle relative architetture. Fu anche lo sviluppatore della tecnologia MOS con porta di silicio (*MOS silicon gate technology*), che permise la fabbricazione dei primi microprocessori e delle memorie EPROM e RAM dinamiche e sensori CCD, gli elementi essenziali per la digitalizzazione dell'informazione.
Nel 1974 fondò e diresse la ditta Zilog,[2] la prima ditta dedicata esclusivamente ai microprocessori, presso cui dette vita al famoso microprocessore Z80, tuttora in produzione. Nel 1986 Faggin co-fondò e diresse la Synaptics, ditta che sviluppò i primi Touchpad e Touch screen.

The First microcomputer



Microsoft Basic

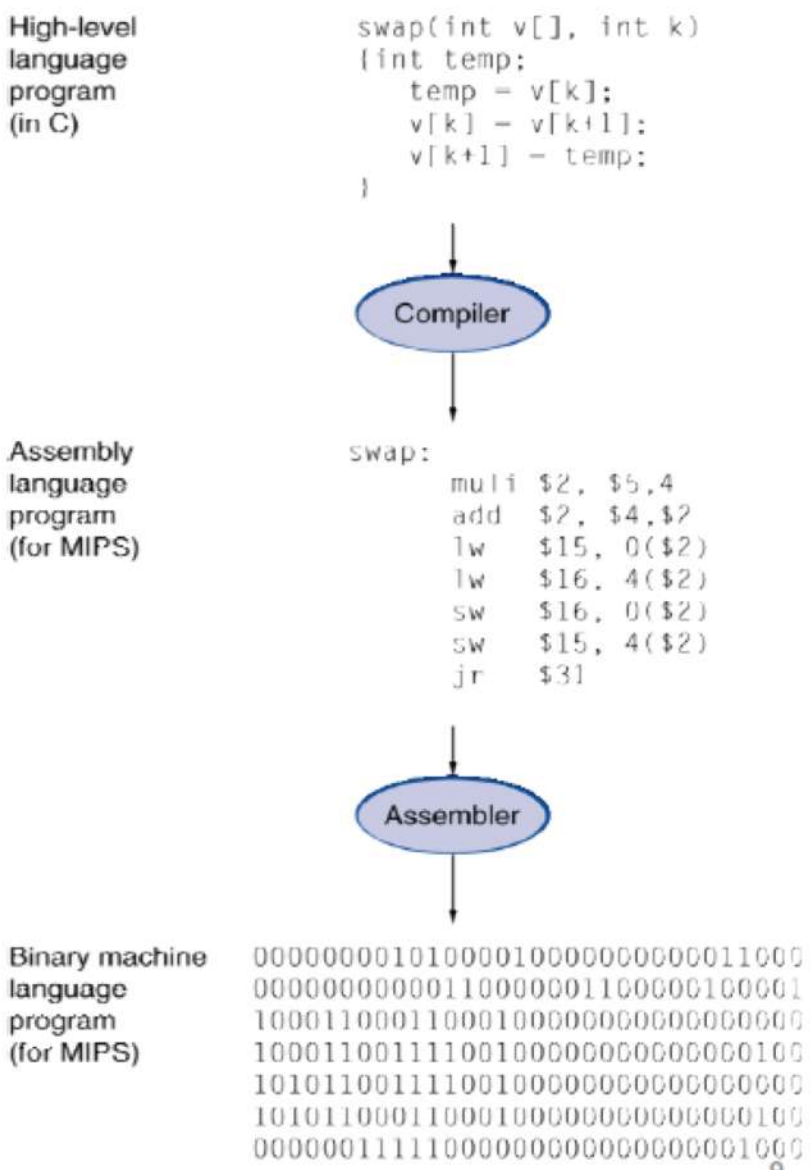
Livelli di astrazione di un architettura di calcolo



- Un architettura di calcolo puo' essere scomposta in diversi *livelli di astrazione*
- Questa descrizione definisce interfacce chiare tra funzionalita' diverse nascondendo i dettagli del singolo livello
    - Un cambiamento di un componente di un certo livello non comporta (non dovrebbe comportare…) cambiamenti negli altri livelli
- L'*astrazione* cresce dai livelli hardware fino al livello applicativo

La gerarchia del codice

- Linguaggio di alto livello
  - "User friendly and intelligible"
  - Assicura produttività e (a volte...) portabilita' tra diverse piattaforme
  - Strumenti software (Compilatore) traducono in assembler (o anche codice eseguibile)
- Linguaggio Assembler
  - Rappresentazione testuale, mnemonica delle istruzioni di un computer
  - Strumenti SW (*Assembler*) traducono "assembly code" nel linguaggio dell'Hardware
- Rappresentazione Hardware
  - Linguaggio Macchina dove le istruzioni ed i dati sono rappresentati da stringhe di bit



1976 Homebrew Computer Club

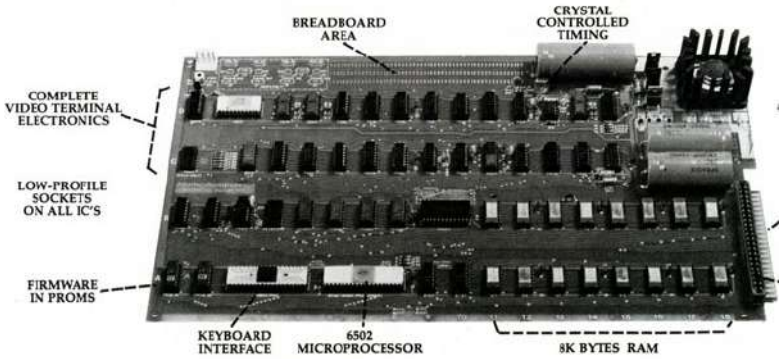
SLAC National Accelerator Laboratory

The Homebrew Computer Club (1978)

available for user programs. And the 16K chips when they become availa- **invited.**

Byte into an Apple **$666.66***

* includes 4K bytes RAM



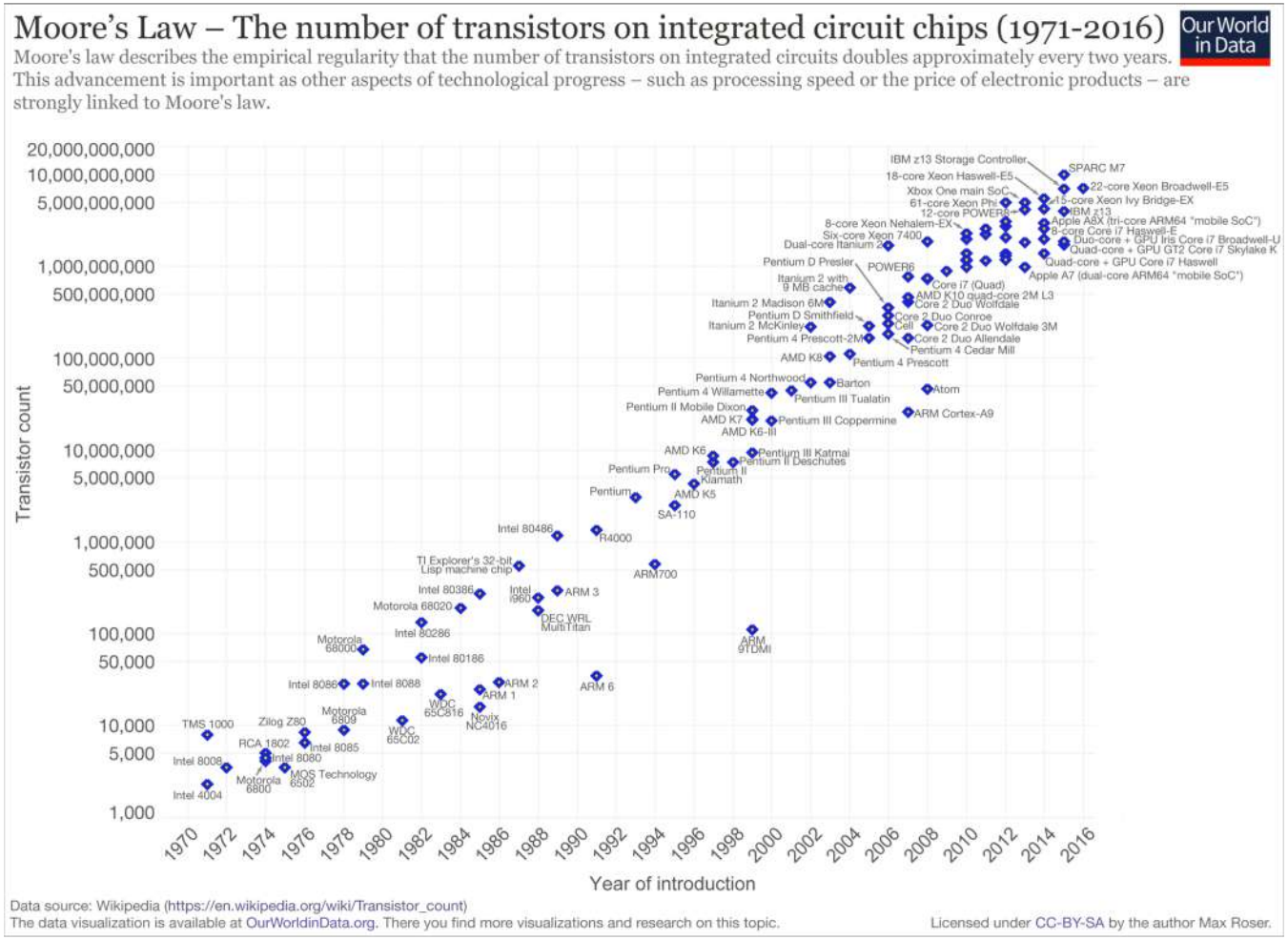
APPLE Computer Company • 770 Welch Rd., Palo Alto, CA 94304 • (4

OCTOBER 1976

CIRCLE NO. 7 ON INQUIRY CARD

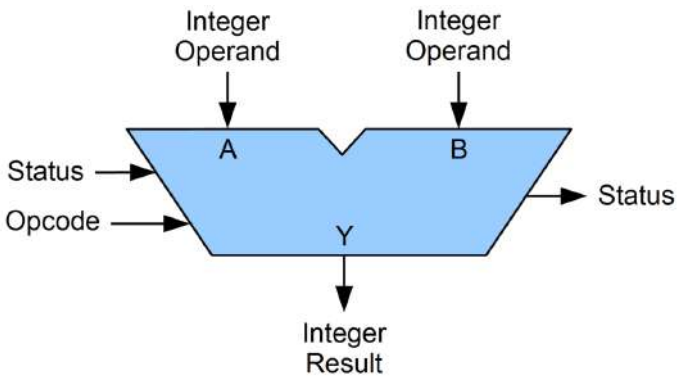
Computer e tecnologia

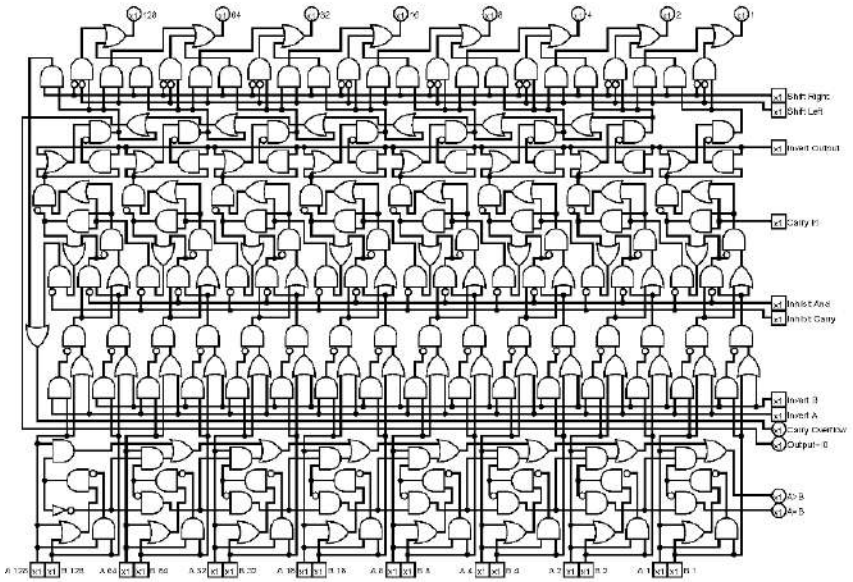
Legge di Moore



Prima legge di Moore (enunciata nel 1971): la complessità di un microcircuito, misurata ad esempio tramite il numero di transitor per chip, raddoppia ogni 18 mesi.

ALU (Arithmetic Logic Unit)

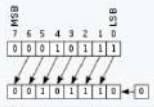
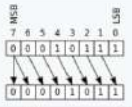
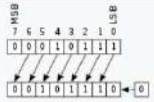
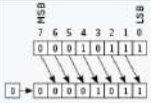
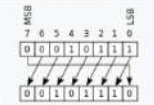
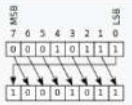
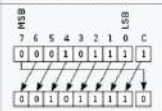
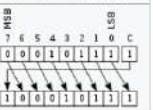




Opcode example

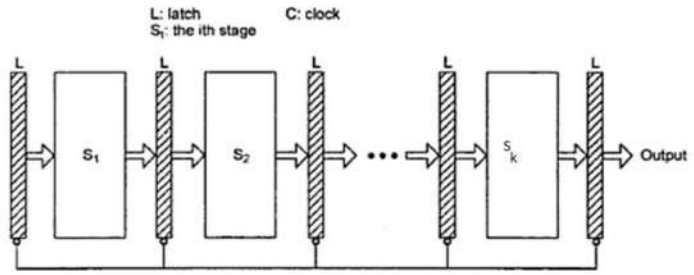
Operation	Description	Opcode, *Op*	Formula
ADD	Add without carry	0 0 0 0	$Y = A + B$
ADC	Add with carry	0 0 0 1	$Y = A + B + C_I$
SUB	Subtractions without borrow	0 0 1 0	$Y = A + \overline{B} + 1$
SBB	Subtractions with borrow	0 0 1 1	$Y = A + \overline{B} + \overline{C_I}$
INC	Increment	0 1 0 0	$Y = A + 1$
DEC	Decrement	0 1 0 1	$Y = A + \overline{1} + 1$
NEG	Negation	0 1 1 0	$Y = 0 + \overline{A} + 1$
NOT	Bitwise complement	0 1 1 1	$Y = \overline{A}$
AND	Bitwise conjunction	1 0 0 0	$Y = A \cdot B \quad (A \wedge B)$
OR	Bitwise disjunction	1 0 0 1	$Y = A + B \quad (A \vee B)$
XOR	Bitwise exclusive disjunction	1 0 1 0	$Y = A \oplus B \quad (A \veebar B)$

Bit shift examples for an eight-bit ALU

Type	Left	Right
Arithmetic shift		
Logical shift		
Rotate		
Rotate through carry		

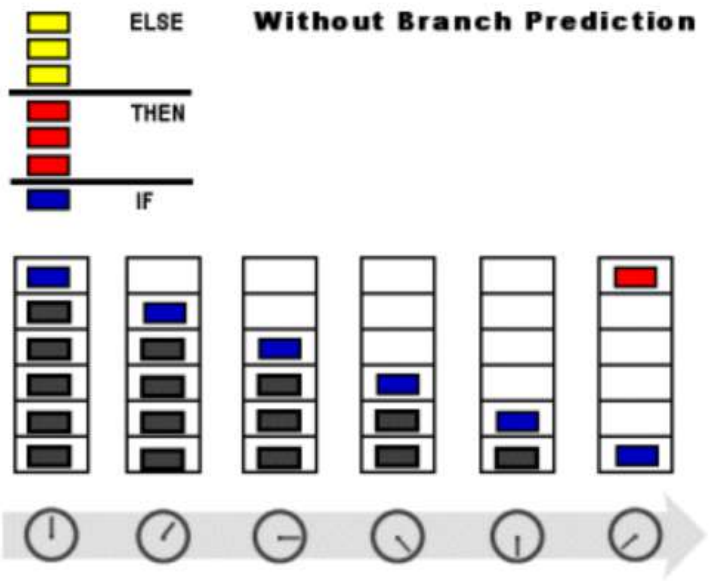
Pipeline

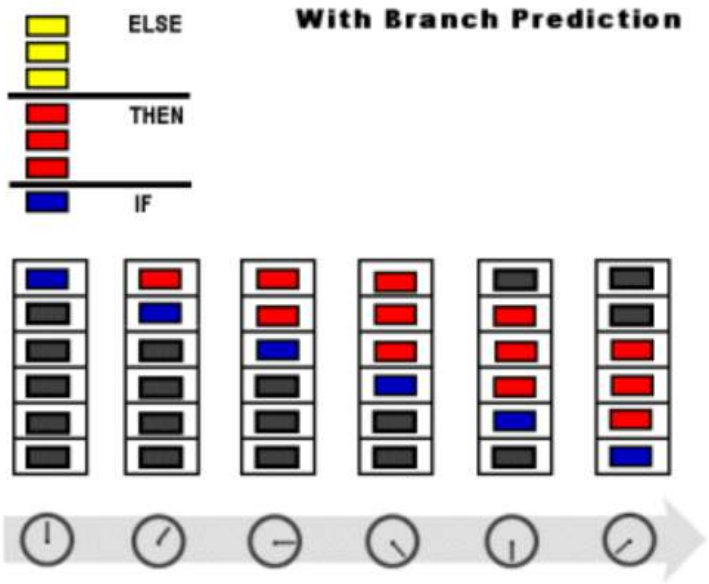
Basic Linear Pipeline



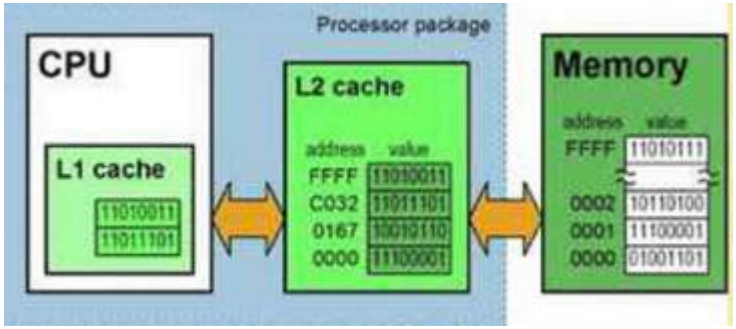
- L: latches, interface between different stages of pipeline
- S1, S2, etc. : pipeline stages

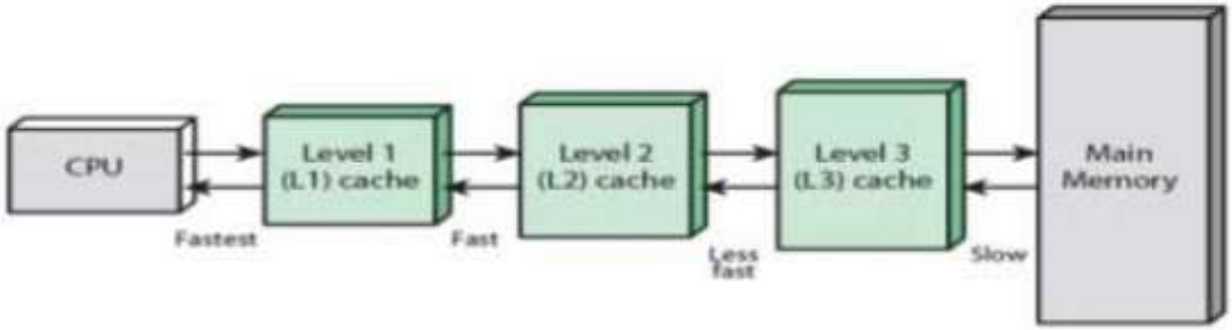
Branch Prediction logic





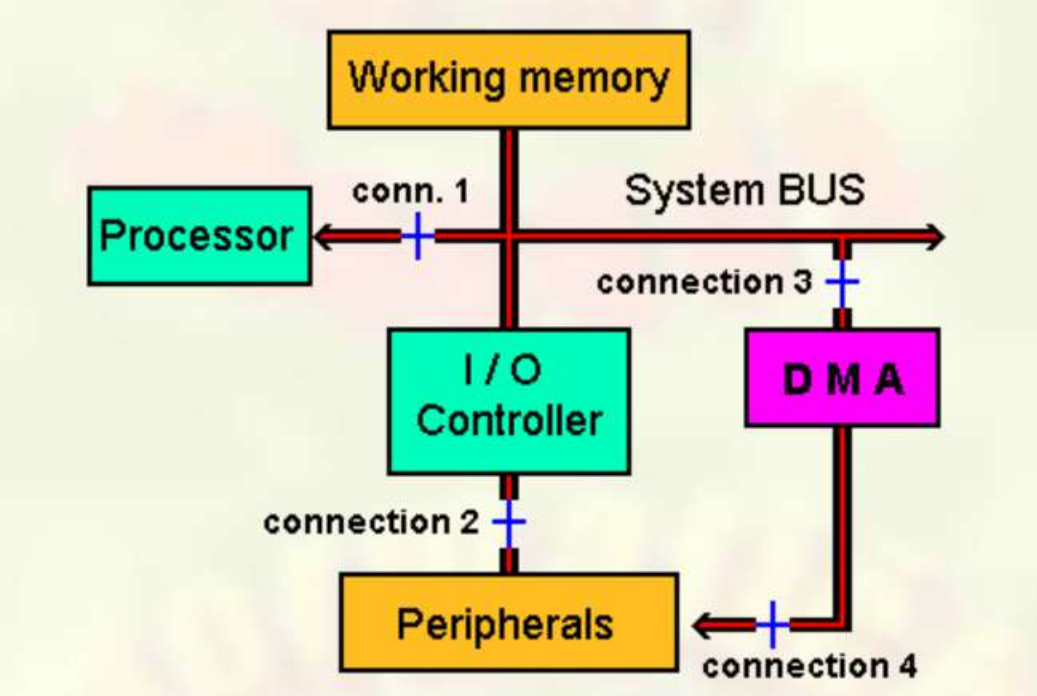
Cache Memory





(b) Three-level cache organization

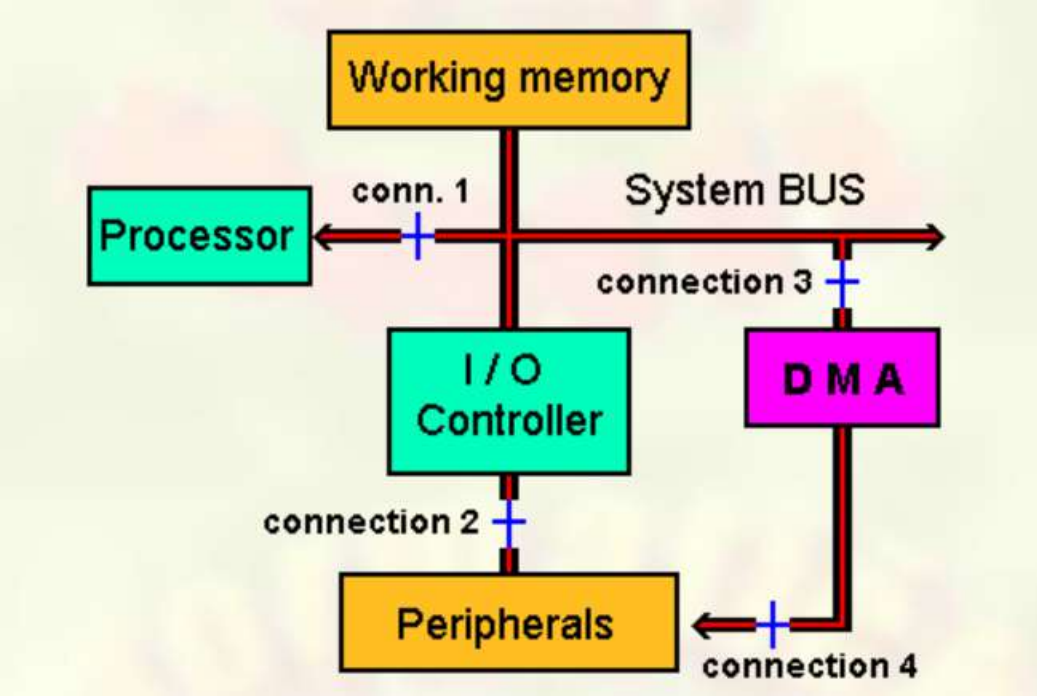
DMA (Direct Memory Access)



DMA

Meccanismo che permette ad altri sottosistemi, quali ad esempio le periferiche, di accedere direttamente alla memoria interna per scambiare dati

DMA (Direct Memory Access)



DMA

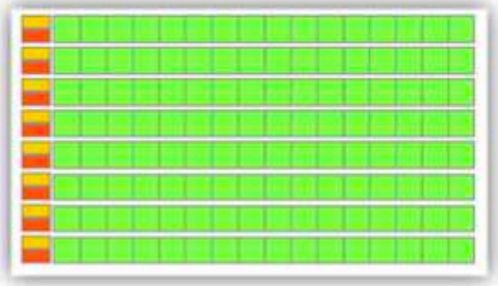
Meccanismo che permette ad altri sottosistemi, quali ad esempio le periferiche, di accedere direttamente alla memoria interna per scambiare dati

CPU vs GPU

CPU

* Low compute density
* Complex control logic
* Large caches (L1$/L2$, etc.)
* Optimized for serial operations
  - Fewer execution units (ALUs)
  - Higher clock speeds
* Shallow pipelines (<30 stages)
* Low Latency Tolerance
* Newer CPUs have more parallelism

GPU



* High compute density
* High Computations per Memory Access
* Built for parallel operations
  - Many parallel execution units (ALUs)
  - Graphics is the best known case of parallelism
* Deep pipelines (hundreds of stages)
* High Throughput
* High Latency Tolerance
* Newer GPUs:
  - Better flow control logic (becoming more CPU-like)
  - Scatter/Gather Memory Access
  - Don't have one-way pipelines anymore

Now (2018)

CPU	Pentium Pro	5,500,000[17]	1995	Intel	500 nm	307 mm²
GPU	GV100 Volta	21,100,000,000[65]	2017	Nvidia	12 nm	815 mm²
CPU	Apple A10X Fusion (hexa-core ARM64 "mobile SoC")	3,300,000,000[51]	2017	Apple	10 nm	96.40 mm²
CPU	72-core Xeon Phi	8,000,000,000	2016	Intel	14 nm	683 mm²
CPU	32-core AMD Epyc	19,200,000,000	2017	AMD	14 nm	768 mm²
GPU	GC2 IPU	23,600,000,000	2018	Graphcore	16 nm	825 mm²

SAPIENZA
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