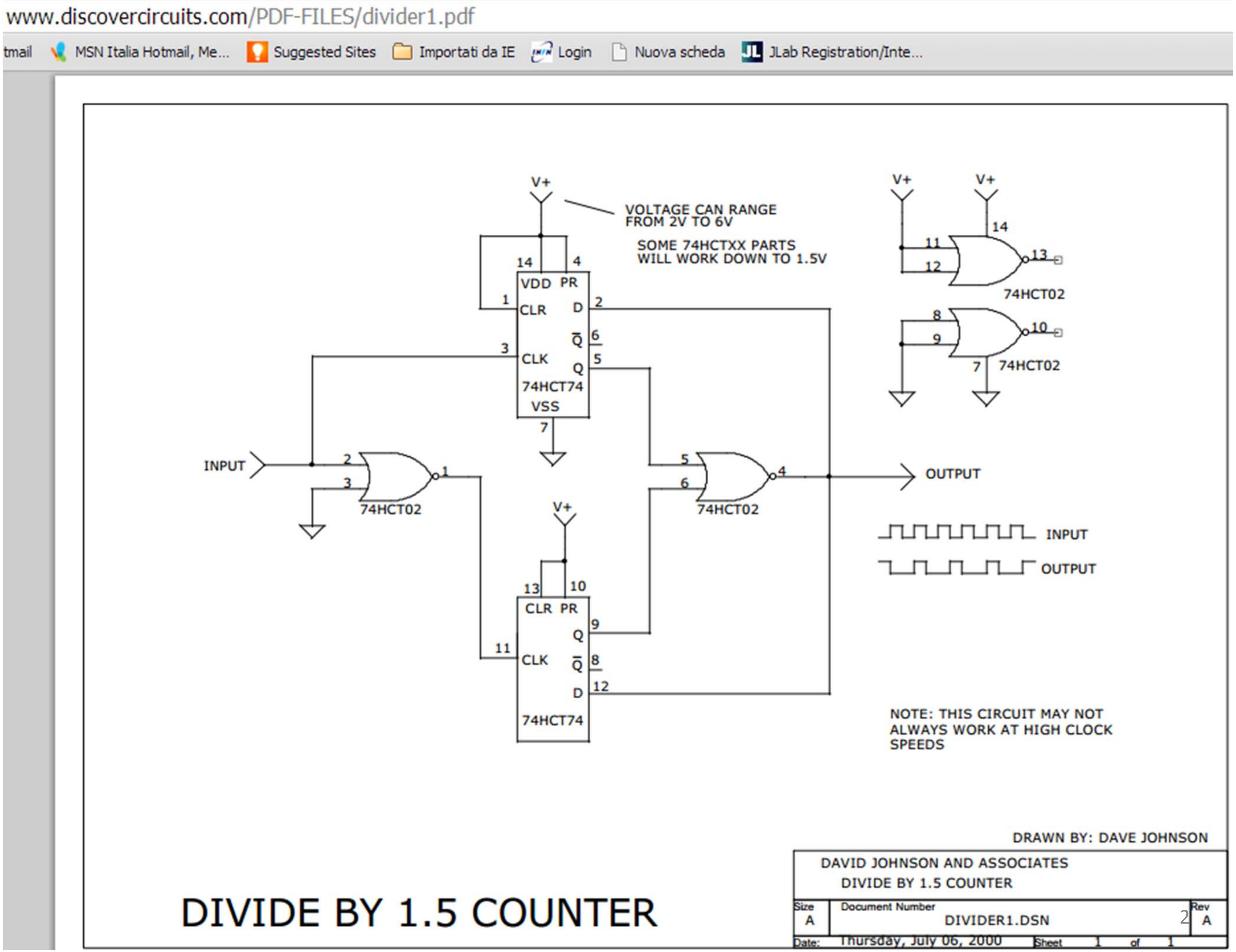
CIRCUIT FORMS DIVIDE BY 1.5 COUNTER

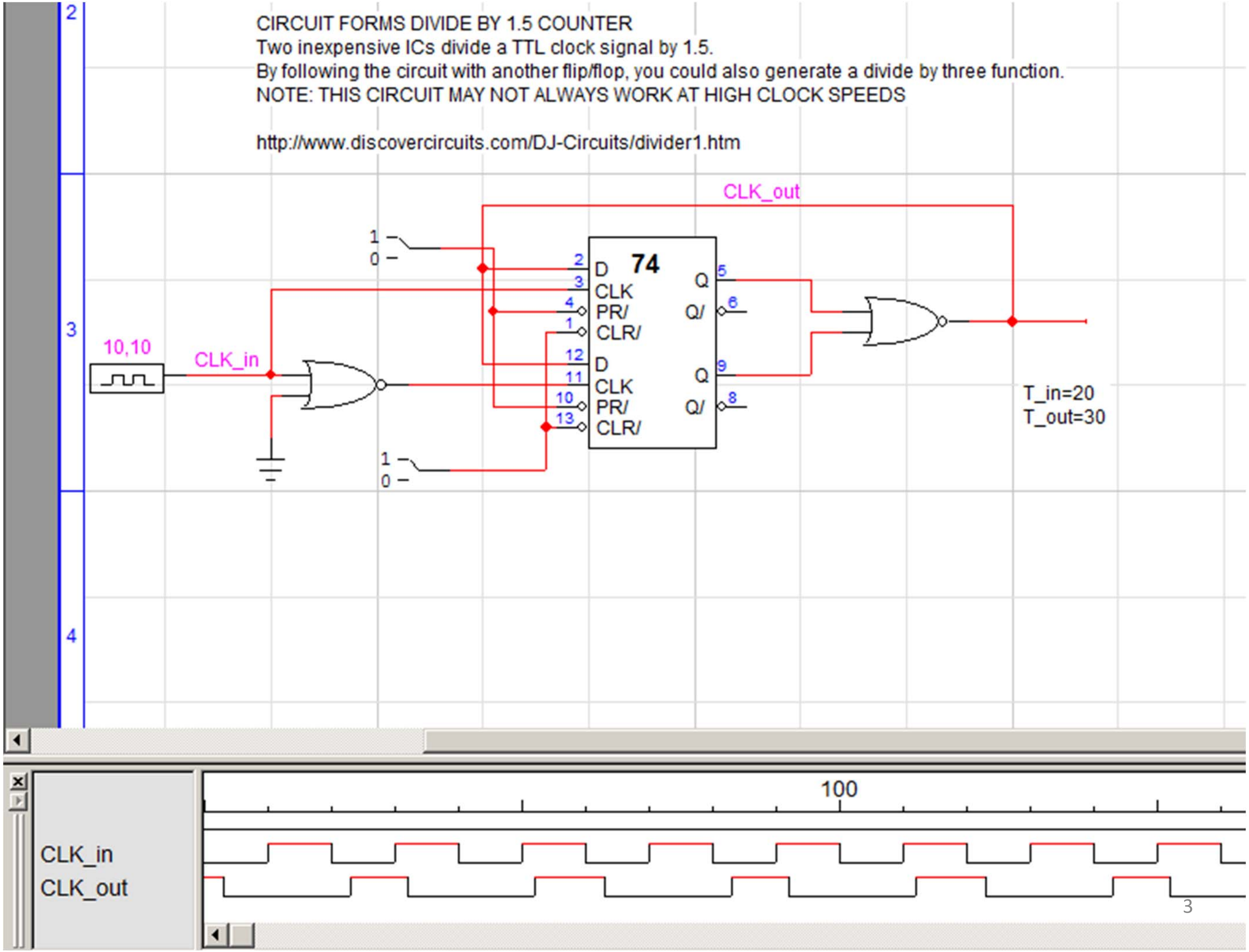
- Two inexpensive ICs divide a TTL clock signal by 1.5.

- By following the circuit with another flip/flop, you could also generate a divide by three function.

NOTE:
THIS CIRCUIT MAY NOT ALWAYS WORK AT HIGH CLOCK SPEEDS

http://www.discovercircuits.com/DJ-Circuits/divider1.htm


www.discovercircuits.com/PDF-FILES/divider1.pdf
tmail MSN Italia Hotmail, Me... Suggested Sites Importati da IE Login Nuova scheda JLab Registration/Inte...
V+
VOLTAGE CAN RANGE FROM 2V TO 6V
SOME 74HCTXX PARTS WILL WORK DOWN TO 1.5V
VDD PR
CLR D
CLK Q̄ Q
74HCT74
VSS
74HCT02
INPUT
OUTPUT
CLR PR
74HCT74
NOTE: THIS CIRCUIT MAY NOT ALWAYS WORK AT HIGH CLOCK SPEEDS
DRAWN BY: DAVE JOHNSON
DAVID JOHNSON AND ASSOCIATES
DIVIDE BY 1.5 COUNTER
Size A
Document Number DIVIDER1.DSN
Rev A
Date: Thursday, July 06, 2000
Sheet 1 of 1
DIVIDE BY 1.5 COUNTER


CIRCUIT FORMS DIVIDE BY 1.5 COUNTER
Two inexpensive ICs divide a TTL clock signal by 1.5.
By following the circuit with another flip/flop, you could also generate a divide by three function.
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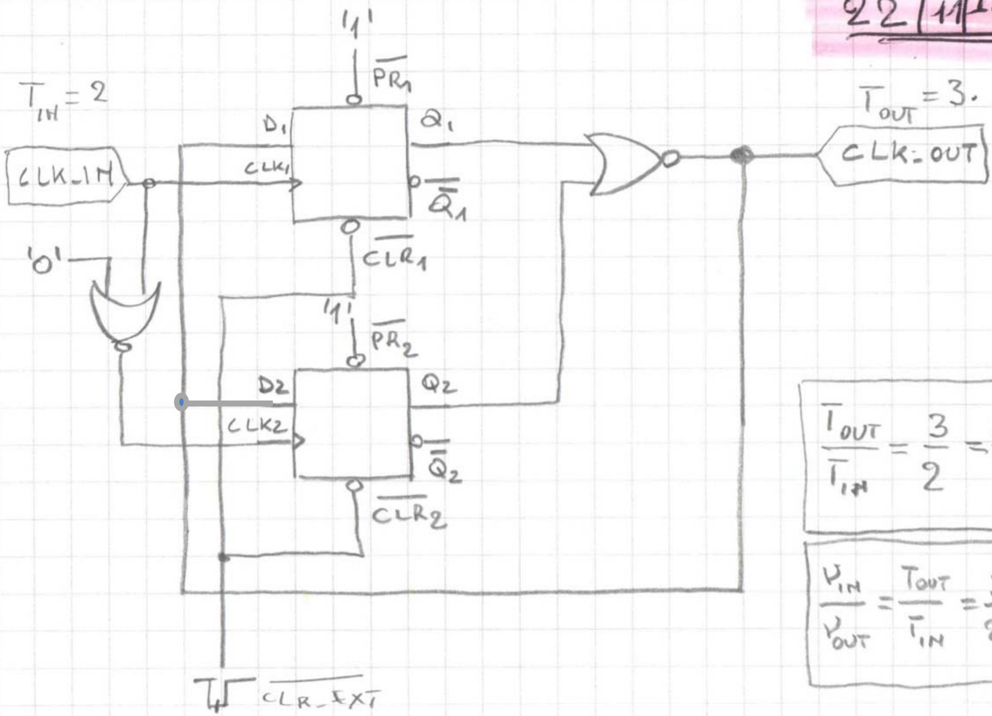
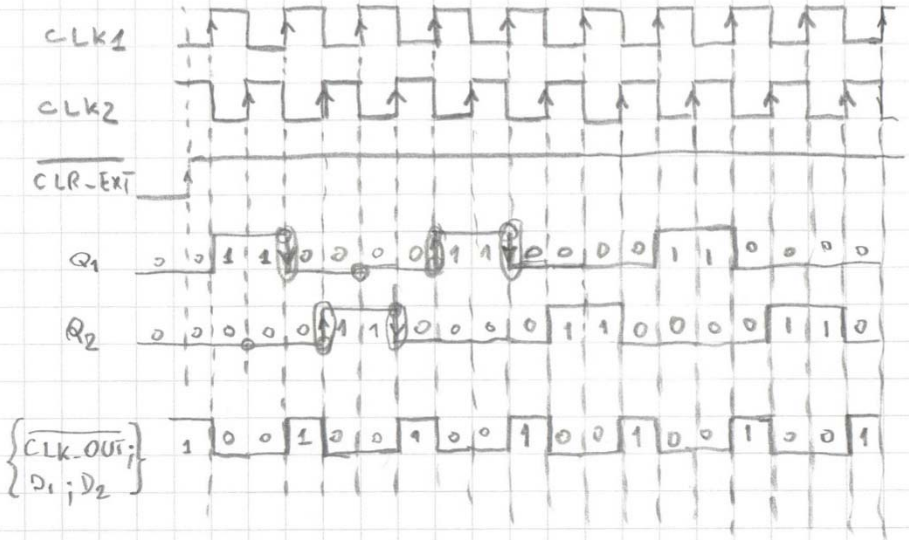
http://www.discovercircuits.com/DJ-Circuits/divider1.htm
CLK_out
74
D
CLK
PR/
CLR/
Q
Q/
10,10
CLK_in
T_in=20
T_out=30
100
CLK_in
CLK_out

22/11/14

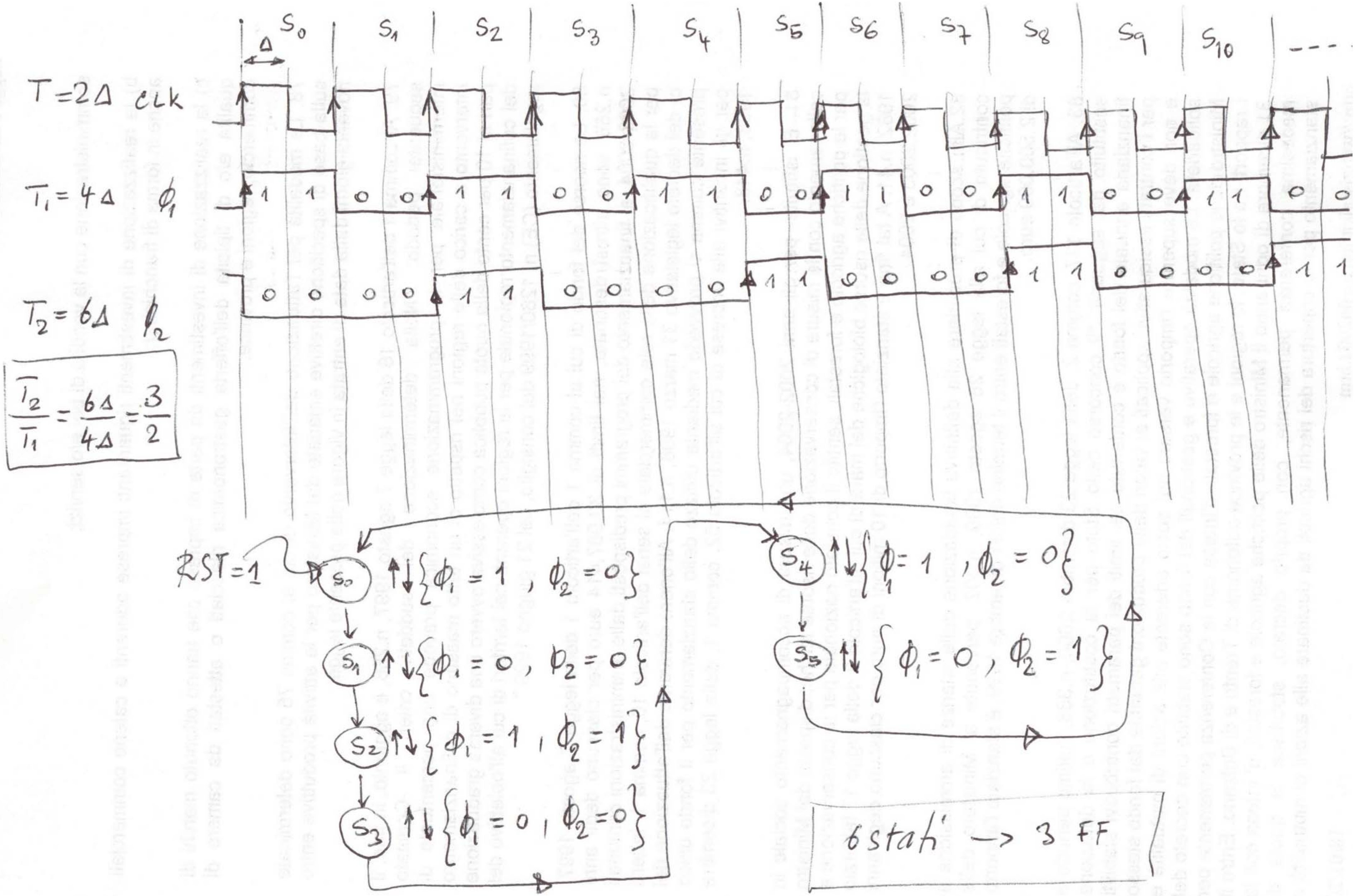


$$\frac{T_{OUT}}{T_{IN}} = \frac{3}{2} = 1,5$$

$$\frac{\nu_{IN}}{\nu_{OUT}} = \frac{T_{OUT}}{T_{IN}} = \frac{3}{2} = 1,5$$



http://www.discovercircuits.com/DJ-Circuits-divider1.htm


S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 ---
Δ
T = 2Δ CLK
T1 = 4Δ ϕ1
T2 = 6Δ ϕ2
T2/T1 = 6Δ/4Δ = 3/2
RST = 1
S0 ↑↓{ϕ1 = 1 , ϕ2 = 0}
S1 ↑↓{ϕ1 = 0 , ϕ2 = 0}
S2 ↑↓{ϕ1 = 1 , ϕ2 = 1}
S3 ↑↓{ϕ1 = 0 , ϕ2 = 0}
S4 ↑↓{ϕ1 = 1 , ϕ2 = 0}
S5 ↑↓{ϕ1 = 0 , ϕ2 = 1}
6 stati → 3 FF

@ t_n			@ t_{n+1}			@ t_n		@ t_n		
Q^A	Q^B	Q^C	Q^A	Q^B	Q^C	ϕ_1	ϕ_2	D^A	D^B	D^C
0	0	0	0	0	1	1	0	0	0	1
0	0	1	0	1	0	0	0	0	1	0
0	1	0	0	1	1	1	1	0	1	1
0	1	1	1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0	1	0	1
1	0	1	0	0	0	0	1	0	0	0
1	1	0	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x

Q^AQ^B \ Q^C	0	1
00	0	0
01	0	1
11	x	x
10	1	0

$D^A = Q^A \cdot \overline{Q^C} + Q^B \cdot Q^C$

Q^AQ^B \ Q^C	0	1
00	0	1
01	1	0
11	x	x
10	0	0

$D^B = Q^B \cdot \overline{Q^C} + \overline{Q^A} \cdot \overline{Q^B} \cdot Q^C$

Q^AQ^B \ Q^C	0	1
00	1	0
01	1	0
11	x	x
10	1	0

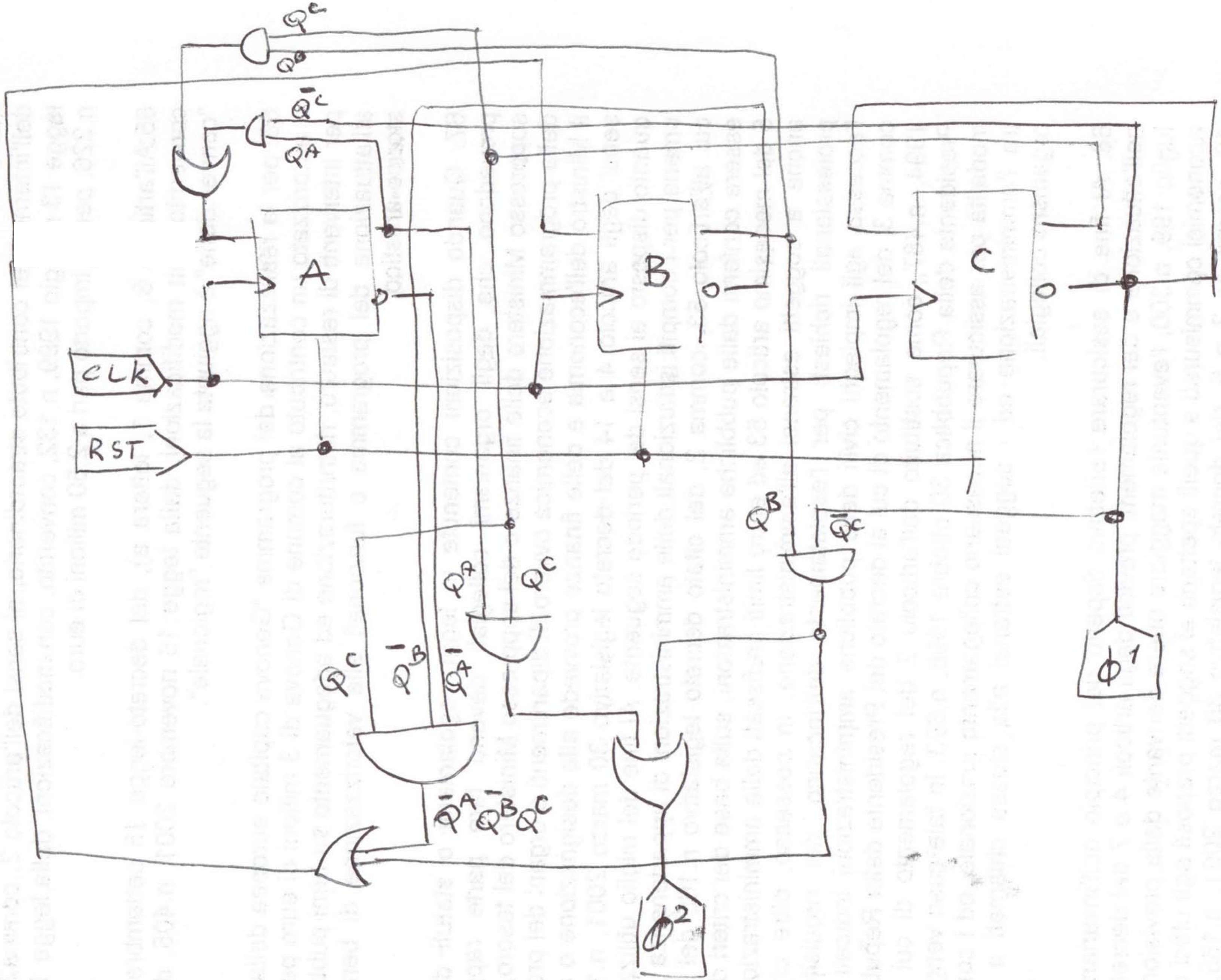
$D^C = \overline{Q^C}$

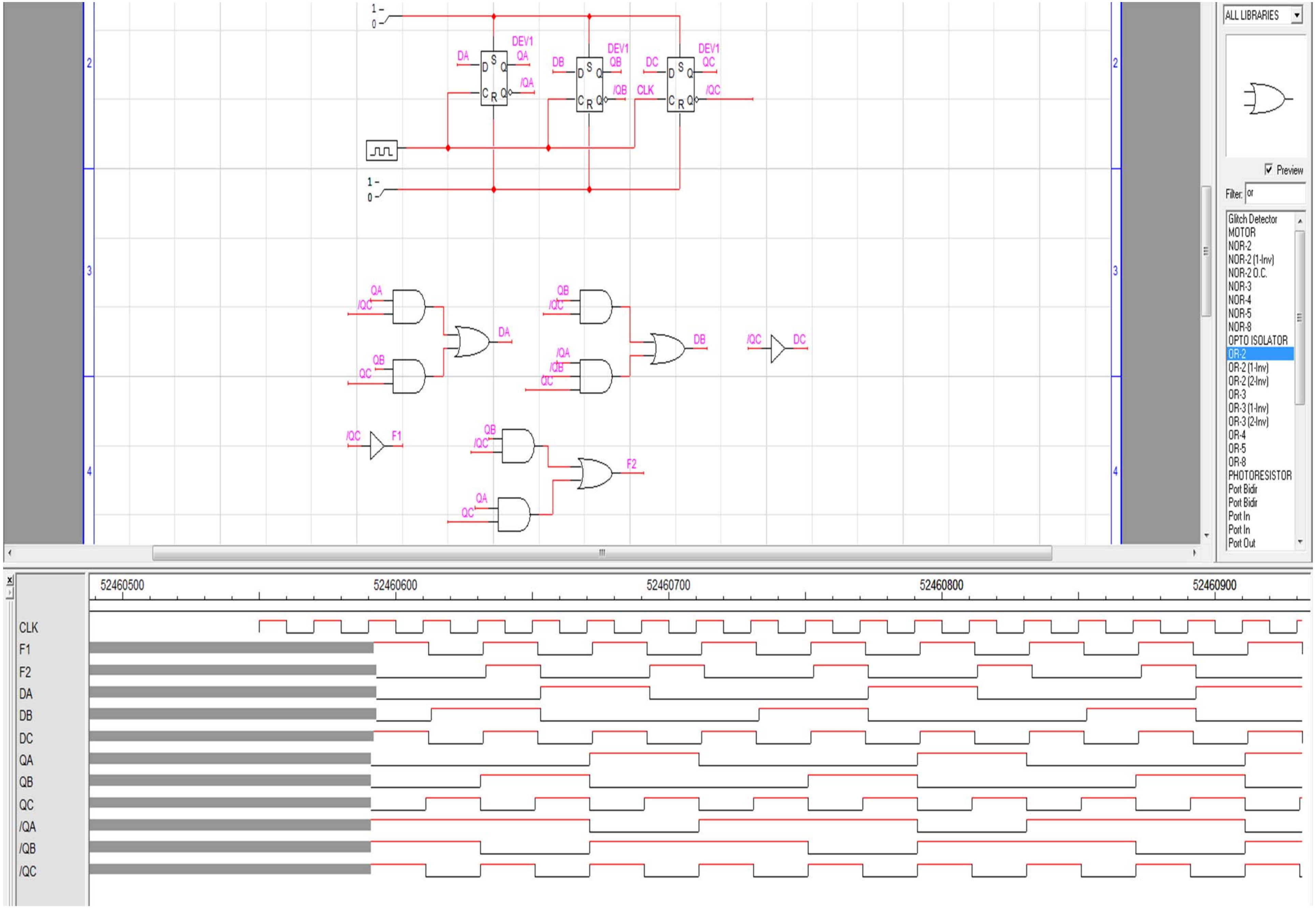
Q^AQ^B \ Q_C	0	1
00	1	0
01	1	0
11	x	x
10	1	0

$\phi^1 = \overline{Q_C}$

Q^AQ^B \ Q^C	0	1
00	0	0
01	1	0
11	x	x
10	0	1

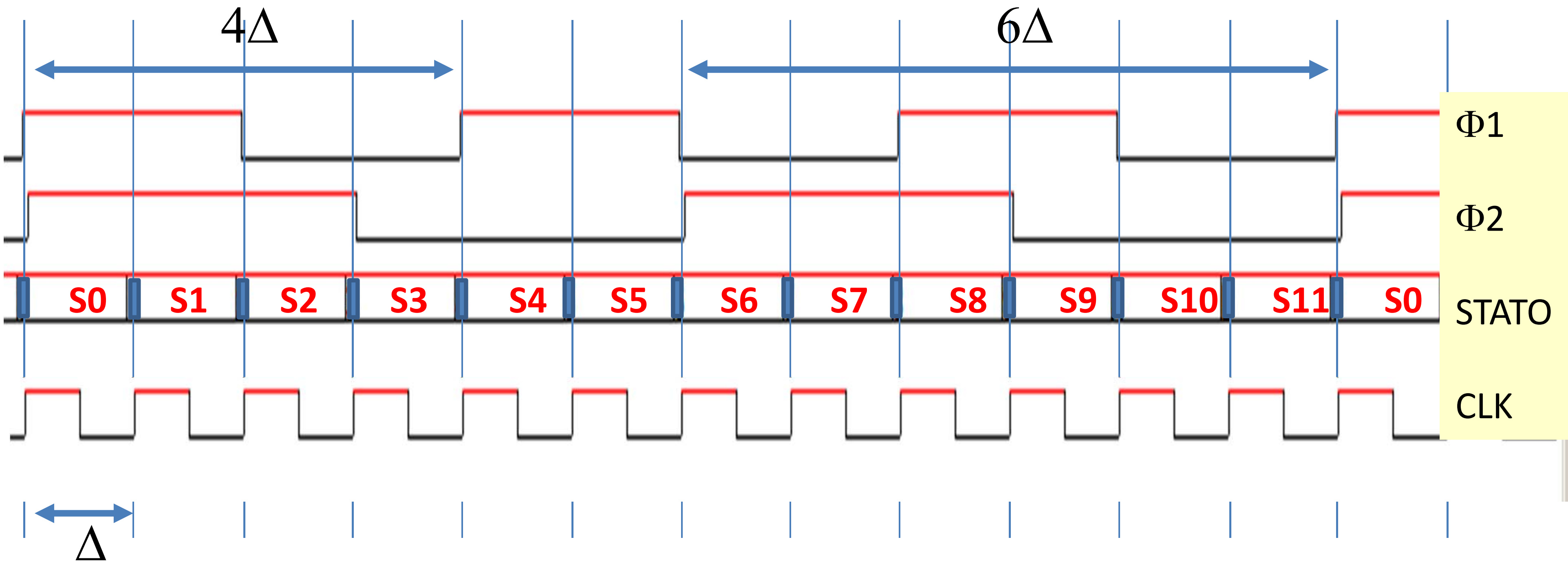
$\phi^2 = Q^B \cdot \overline{Q^C} + Q^A \cdot Q^C$


A
B
C
CLK
RST
Q^C
Q^B
$\bar{Q}^C$
Q^A
Q^B
$\bar{Q}^C$
Q^A
Q^C
Q^C
$\bar{Q}^B$
$\bar{Q}^A$
$\bar{Q}^A\bar{Q}^BQ^C$
ϕ^1
ϕ^2


DEV1
DA
QA
/QA
DB
QB
/QB
DC
QC
/QC
CLK
F1
F2
ALL LIBRARIES
Preview
Filter: or
Glitch Detector
MOTOR
NOR-2
NOR-2 (1-Inv)
NOR-2 O.C.
NOR-3
NOR-4
NOR-5
NOR-8
OPTO ISOLATOR
OR-2
OR-2 (1-Inv)
OR-2 (2-Inv)
OR-3
OR-3 (1-Inv)
OR-3 (2-Inv)
OR-4
OR-5
OR-8
PHOTORESISTOR
Port Bidir
Port Bidir
Port In
Port In
Port Out
52460500
52460600
52460700
52460800
52460900

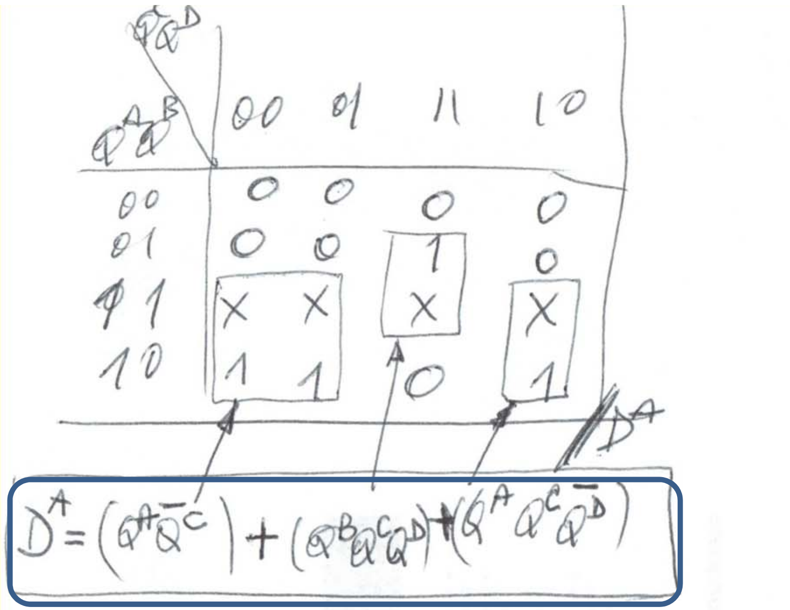
Come ottenere un duty-cycle del 50% nel divisore della frequenza del clock secondo un rapporto

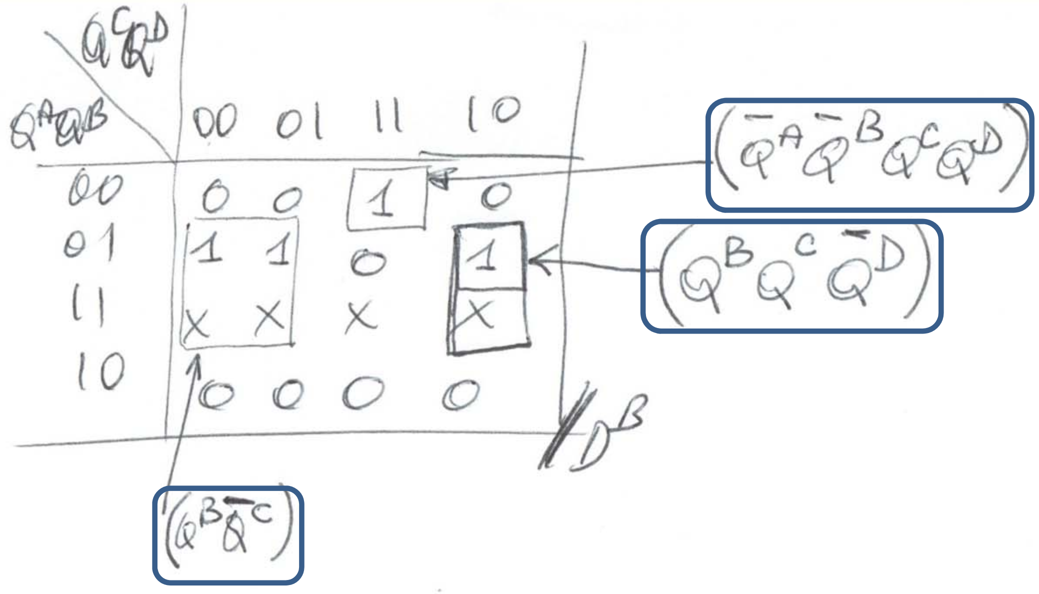
3 : 2

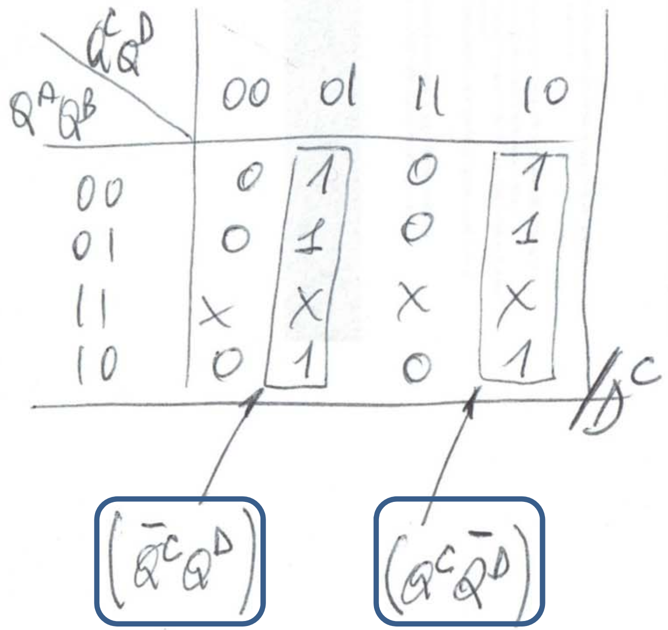


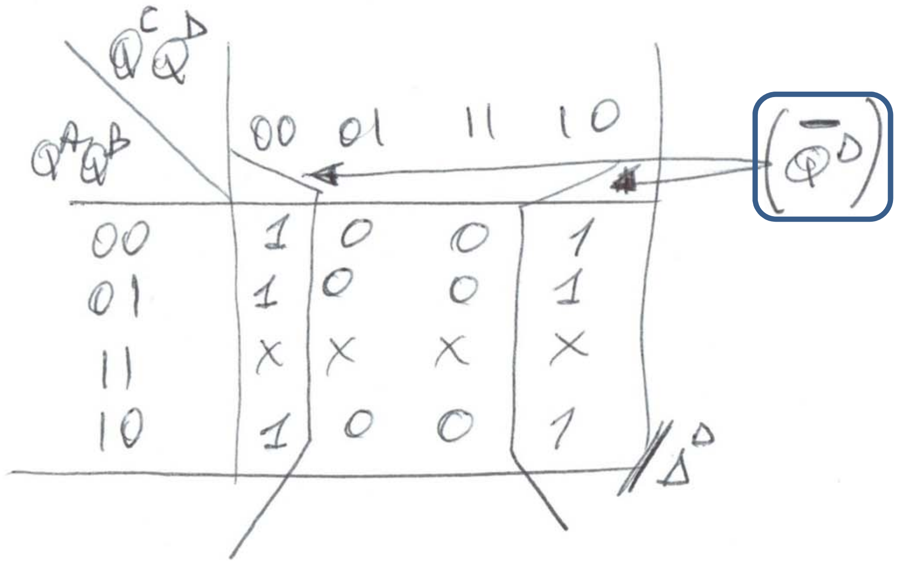
FSM: # 12 STATI ←→ # 4 Flip-Flop

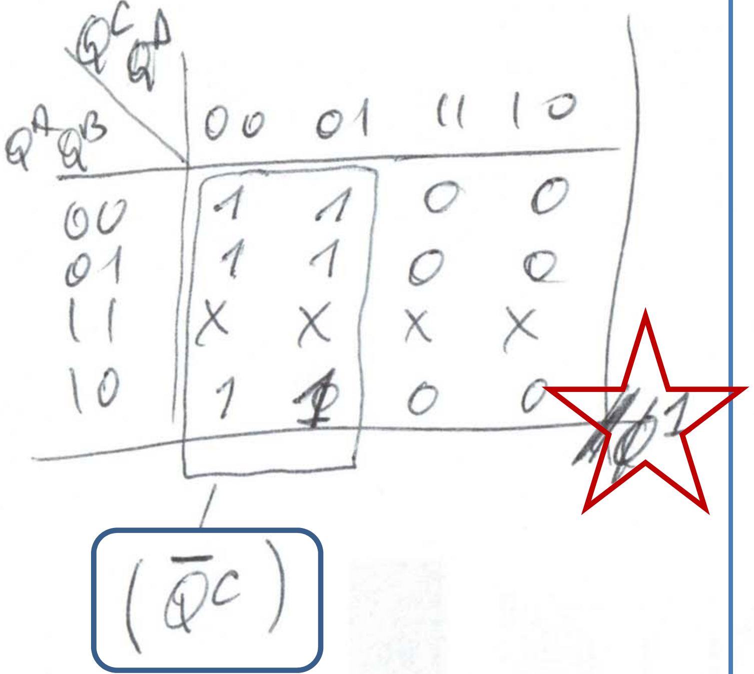
	@ tn				@ tn+1				@ tn		@ tn			
	Q^A	Q^B	Q^C	Q^D	Q^A	Q^B	Q^C	Q^D	ϕ^1	ϕ^2	D^A	D^B	D^C	D^D
S_0	0	0	0	0	0	0	0	1	1	1	0	0	0	1
S_1	0	0	0	1	0	0	1	0	1	1	0	0	1	0
S_2	0	0	1	0	0	0	1	1	0	1	0	0	1	1
S_3	0	0	1	1	0	1	0	0	0	0	0	1	0	0
S_4	0	1	0	0	0	1	0	1	1	0	0	1	0	1
S_5	0	1	0	1	0	1	1	0	1	0	0	1	1	0
S_6	0	1	1	0	0	1	1	1	0	1	0	1	1	1
S_7	0	1	1	1	1	0	0	0	0	1	1	0	0	0
S_8	1	0	0	0	1	0	0	1	1	1	1	0	0	1
S_9	1	0	0	1	1	0	1	0	1	0	1	0	1	0
S_{10}	1	0	1	0	1	0	1	1	0	0	1	0	1	1
S_{11}	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	1	1	0	0	X	X	X	X	X	X	X	X	X	X
	1	1	0	1	X	X	X	X	X	X	X	X	X	X
	1	1	1	0	X	X	X	X	X	X	X	X	X	X
	1	1	1	1	X	X	X	X	X	X	X	X	X	X

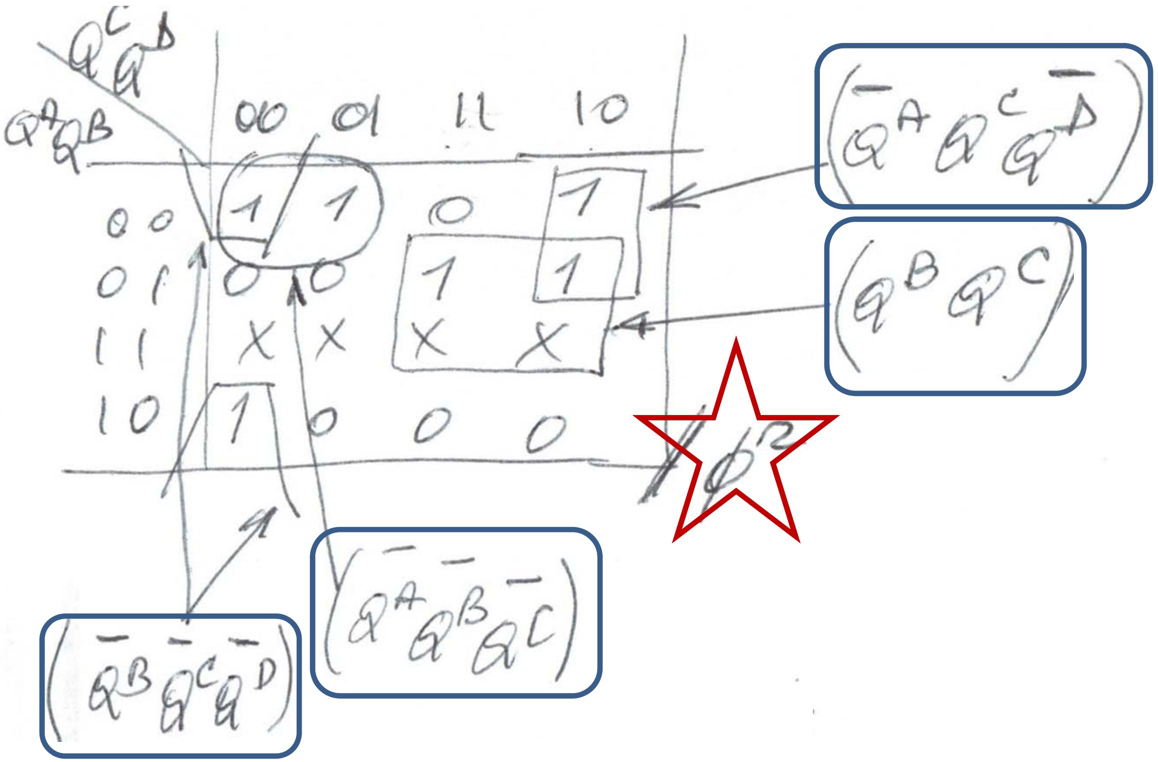

$Q^C Q^D$
$Q^A Q^B$
00 01 11 10
D^A
$D^A = (Q^A \bar{Q}^C) + (Q^B Q^C Q^D) + (Q^A Q^C \bar{Q}^D)$

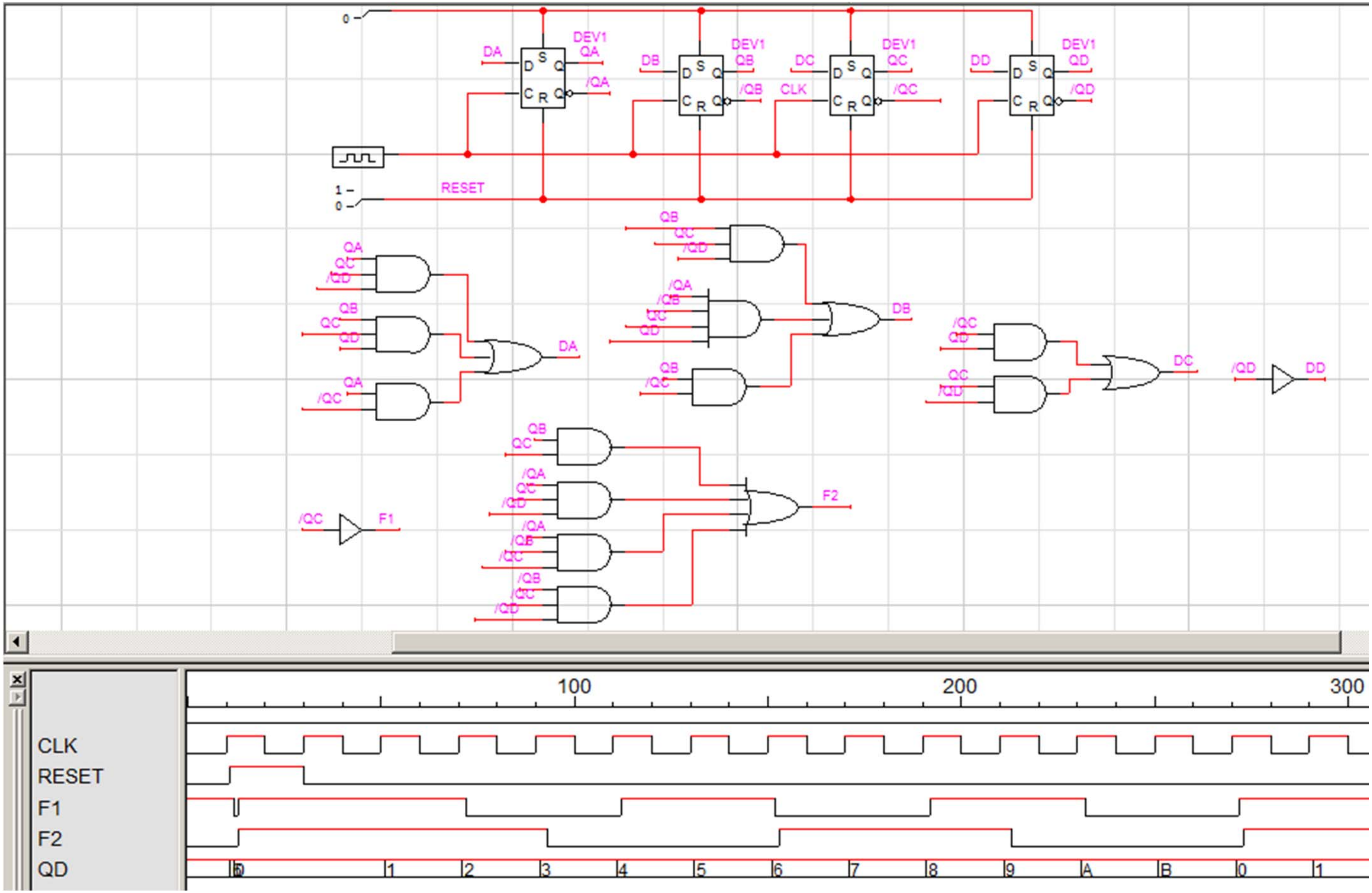

$Q^C Q^D$
$Q^A Q^B$
00 01 11 10
D^B
$(\bar{Q}^A \bar{Q}^B Q^C Q^D)$
$(Q^B Q^C \bar{Q}^D)$
$(Q^B \bar{Q}^C)$


$Q^C Q^D$
$Q^A Q^B$
00 01 11 10
D^C
$(\bar{Q}^C Q^D)$
$(Q^C \bar{Q}^D)$


$Q^C Q^D$
$Q^A Q^B$
00 01 11 10
D^D
$(\bar{Q}^D)$


QC QD
QA QB
00 01 11 10
00 01 11 10
$(\overline{Q^C})$


QC QD
QA QB
00 01 11 10
00 01 11 10
$(\overline{Q^A} Q^C \overline{Q^D})$
$(Q^B Q^C)$
$(\overline{Q^B}\,\overline{Q^C}\,\overline{Q^D})$
$(\overline{Q^A}\,\overline{Q^B}\,\overline{Q^C})$



DEV1
DA
QA
/QA
DB
QB
/QB
DC
QC
/QC
CLK
DD
QD
/QD
RESET
F1
F2
100
200
300
CLK
RESET
F1
F2
QD