Test Station for the LHCb Muon Front-End Boards (November 2005)


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Abstract - The INFN LHCb group in Rome has developed and implemented hardware and software of a fixture to test LHCb Muon Front-End (FE) circuitry for MWPC and GEM chambers. Front-End boards are made up of two Amplifying, Shaping and Discriminating (ASD) ASICs and a read-out and control ASIC, all of which accessible via an I2C based data transfer protocol. The resulting testing station allows bench tests of front-end readout circuitry using the same facilities which will be available for their supervision, as well as a 16-channel charge injector, a custom read-out board, and a Win API C++ program (to control and analyze data) developed especially for this purpose. The outcome is a user friendly system which will be widely utilized in the course of chambers and readout electronics tests, and during the installation phase of the experiment. The main relevant aspects of quality assurance are: data transfer, board connectivity, sensitivity, offset and noise. A Time to Digital converting component has also been implemented in order to evaluate the output signals' timing response of the Device Under Test (DUT). A brief summary of preliminary results obtained during its development and implementation is also featured.

Index Terms - Front-end, charge injection, quality control, converter, automation, readout, calibration.

I. INTRODUCTION

HCb Muon chambers and their read-out electronics have entered production phase this year. All subsystems and parts should be thoroughly tested at different locations before becoming part of the LHCb apparatus; some of the institutes which will use and test those chambers and circuits are: CERN (Geneva), LNF (Frascati, Italy) and INFN (Cagliari, Italy). Test equipment [1] thought for this purpose aims at achieving the highest test coverage at the lowest cost, and should be easy to replicate, to transport and operate. Moreover, data acquisition should be simple and reliable; it can be performed via a USB connection or with final supervisory and control equipment of the Muon LHCb System, already in use at several institutes.

For a functional test of fully-fitted FEBs which will eventually be part of the LHCb Muon System [2], as many as 7 different procedures have been evaluated for both their digital and analog characteristics. The parameters to be considered are: on-board component connectivity, circuit noise, sensitivity, offset and timing.

A. Front-End Under Test

The LHCb Muon FE Board is called CARDIAC [3] (CARIoca DIalog Circuit); it is composed of 2 ASD chips (CARIOCA) and a third chip (DIALOG) with features for diagnostics, timing adjustment and logic. Two versions of CARDIAC have been designed, in order to be able to operate also with Triple-GEM chambers.

Fig. 1. CARDIAC schematic diagram

CARIOCA [4] (Cern And RIO Current-mode Amplifier) is an IBM 0.25μm CMOS ASIC developed for data readout of the LHCb Muon Detector. Such an ASIC holds 8 identical current-mode ASDB (Amplifier, Shaper Discriminator, Baseline restorer) channels with individual threshold inputs. CARIOCA has been developed to process MWPC cathode and anode signals (positive and negative polarities) and to accept signals from Triple-GEM detectors as well. CARIOCA has a peaking time of about 10ns, during which the pulse input charge accumulated is converted into a voltage signal. Therefore the test station injection pulse should be completed before CARIOCa's peaking time.

DIALOG [5] is an ASIC developed with the same IBM process as CARIOCA, and its main task is to generate logical channels from physical channels received from ADS’s, carrying out an adjustment in time and width of physical channels, and performing calibration of all ASD's lines. DIALOG performs calibration using a DAC with increments small enough to permit accurate enough noise measurements even with an equivalent input capacitance of 0pF.

II. TESTS

A. Digital

Digital tests are based on read and write routines to evaluate bit-by-bit response and on auto-injection procedures in order to test the FEB facilities themselves and their internal counters.
B. Analog

1) Connectivity

Board connectivity is tested by means of injection of a charge pulse, having previously adjusted the threshold to a certain value. In this way the entire path from FEB inputs to their outputs is put under test. Such a procedure allows easy and quick identification of failures in assembled boards and therefore it should be executed at the beginning of the analog part of each testing sequence.

2) Equivalent Noise Charge

Due to the presence of noise, for each charge injection the amplifier has a certain statistic distribution. The probability density function describing the amplifier response in the presence of Gaussian noise can be expressed by the formula:

\[ f(V) = Ne^{-\frac{(V-V_m)^2}{2\sigma^2}} \]  

given a discriminator threshold \( V_{th} \), the probability that an input charge \( Q_{in} \) (which is equivalent to \( V_{in} \)) results in a discriminator hit is given by:

\[ P = \int_{-\infty}^{\infty} Ne^{-\frac{(V-V_m)^2}{2\sigma^2}} dV \]  

Such an equation can be represented in terms of the error function:

\[ P = \frac{1}{2} - \frac{1}{2} \text{erf}\left(\frac{V_m - V_m}{\sqrt{2}\sigma}\right) \]  

It can be demonstrated that:

\[ \sigma_n \approx \frac{V_m^{[25\%]} - V_m^{[75\%]}}{1.35} \]  

Taking into account the above considerations it can be concluded that an efficiency of 50% gives the injected charge equivalent threshold (true threshold).

In actual practice, the efficiency curve is obtained varying the threshold while a fixed charge is injected. Acquired data can then be fitted and a noise rms figure is obtained in Volts. This value can be subsequently converted into Coulombs once channel sensitivity is known.

3) Sensitivity

Measurements of CARIOCA sensitivity can be made by means of a threshold scan with different injected charges in the range between approximately 2 and 15fC. In this way several s-curves are produced and a Volts per Coulomb sensitivity is obtained.

4) Bias

Bias can be determined in two ways: extrapolating the sensitivity curve and by means of a noise analysis (without injection). The latter allows bias identification by measuring a maximum noise rate during a threshold scan procedure.

The CARIOCA discriminator makes use of a Differential Threshold Voltage (DTV) circuit (8 replicas in total). It can provide a differential threshold (VrefA - VrefB) from a single polarity reference voltage (Vref).
Fig. 4. Differential Threshold Voltage (DTV)

Assuming DTV usage for the CARIOCA discriminator one can expect a mirrored noise rate behavior according to threshold variations as shown in Figure 5. This noise measurement procedure has been implemented to provide and accumulate data for further analysis.

![DTV Diagram](image)

**Fig. 5.** CARIOCA threshold scan and noise rate using DIALOG chip.

The current Test Station uses such a measurement to determine FE circuit bias.

5) **Pulse Width and Time Walk**

A TDC with 81ps of resolution has been implemented in the Control Board circuitry. This system circuitry receives the strobe signal from the injection logic and all the FE output channels. Such a scheme permits measurement of width and time-walk of individual output signals.

![TDC Timing Diagram](image)

**Fig. 6.** TDC timing measurement diagram

III. **SYSTEM**

A. **System Overview**

The main building blocks of test equipment are a charge injector, a read-out and counting device, a Time to Digital Converter (TDC-GPX from ACAM) custom circuit, either a CANbus interface or an USB adaptor and an integrated C++ program.

![System Diagram](image)

**Fig. 7.** FEB Test Station Schematic diagram

B. **Electronics**

The Injection Board (IB) contains 16 channels and its circuitry permits a fine tuning of injected charge (in the range of a few fC) and of ASD threshold values, since CARIOCA has 8 individual threshold inputs. It can also mask out any chosen group of channels, adjust the injection rate and finally inject either positive or negative charge as required.

A Control Board receives differential signals from the CARDIAC under test and processes data by means of 8 counters (all synchronized with IB signals); all the logic functions, as well as the TDC functionality, are implemented on an ACTEL ProAsicPlus FPGA. Data transfer with a host computer takes place via either a CANbus adaptor or an USB interface.

Signals from FEBs are collected by the TDC and features such as time-walk and pulse width are measured by comparison. TDC technical main specifications are: a resolution of 81ps, capability to work with either rising or falling edges, 5.5ns pulse pair resolution with a multi-hit feature. All FPGA internal registers are accessed by an I2C interface, allowing fine tuning of the injected charge as well as a selection of channels to inject and of course supervision of the FEB ASICS through the same mechanism.

Prior to testing each device, the entire system has to be calibrated, as it is meant to be used for automated testing: for this purpose an auto-calibration procedure has also been implemented, performing calibration of injection lines using a known good (KG) FEB. System inputs are bias and sensitivity characteristics of single channels of a KG FEB, which then constitute the conversion values applied to each injection line.
C. Software

A C++ based WinAPI program has been developed to control and to process data, carrying out tests, data analysis and archiving.

Preliminary testing stages are: access to FEB registers and an auto-injection procedure. Once a basic degree of functionality is certain, the software tool can proceed further to help investigate, as shown in Figure 8, several aspects of the device under test: Connectivity, Noise, Sensitivity and Offset.

Fig. 8. A flow chart-like view of the testing process

Finally a proper data acquisition based on the TDC is performed, to measure time-walk and pulse width. Test results of every device are stored in order to allow further analysis, keeping a track of each device in a results database, which will be utilized in due course by the ECS for monitoring purposes.

Fig. 9. User Interface of the Test Suite

To shorten test duration the suite runs in parallel, on four channels at a time.

IV. RESULTS

An initial run of tests was performed, with the aim of assessing system robustness, basic operation and a self-calibration procedure. Using a FEB, the apparatus was successfully calibrated and then the same board was checked again using calibration data gained in the first run 145 more times. Such a method is good to appraise the intrinsic station error (calibrated sensitivity: 15mV/fC and offset 800mV).

Fig. 10. Sensitivity and Offset histograms
Testing of 50 FEB for Triple-GEM detector, in the LHCb Muon Collaboration, has already been performed and results are presented here.

10% of the total amount has been found defective due to short-circuit, communication failures or chip connectivity. The remaining 90% (720 FE channels) has been completed tested as shown by the following histograms.

V. CONCLUSIONS

A self contained test apparatus and a testing methodology for LHCb Muon Front-End electronics have been developed. Results obtained so far have proved to be very accurate and useful in determining faults of FEBs so that more replicas of the fixture are being integrated and will be used for systematic production tests of a proportion of FEBs.

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REFERENCES


Fig. 11. A summary of the most recent test results