The LHCb Muon Control System
The DAQ Domain

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Abstract—The LHCb Muon System consists of 122000 front-end channels, distributed on about 8000 front-end boards (on detector). 152 Off detector boards (each containing 192 channels) gather information from front-end and send it to the DAQ and trigger systems. The Muon System is highly configurable and is conceived to allow a deep control of the behavior of the whole system during data taking. This results in a large number of configuration and status registers to be handled. The Muon Control System, part of the LHCb Experiment Control System, is based on a PVSS II framework and is managed by a hierarchical Finite State Machine. We illustrate the Control System architecture and the characteristics of its components, Control Units and Device Units. We also illustrate system performance in data communication, between the OPC servers and system electronics, obtained through a suitable design of dedicated firmware.

I. INTRODUCTION
The LHCb experiment, now under construction at the Large Hadron Collider (LHC) of the European Organization for Nuclear Research (CERN), is dedicated to the study of CP violation and rare decays in the B meson sector.

The Muon Detector [1] consists of five stations (M1-M5). The five stations are equipped with a total of 1368 Multi-Wire-Proportional-Chambers (MWPC), with the exception of the inner region of station M1, where 24 Gas-Electron-Multipliers (GEM) are used. The Muon Chambers supply binary information on their 122000 read-out channels, arranged on about 8000 Front-end boards (CARDIAC boards), placed on detectors. Each CARDIAC manages 16 front-end channels. The front-end channels undergo some stages of logic reductions (on the CARDIAC and on the IB boards) and are sent to the ODE boards, placed off detector. 152 ODE boards are used in the System. Fig. 1 illustrates a sketch of the Muon System architecture. The Muon System electronics is highly programmable and configurable. Moreover, it is endowed with a large number of status registers and counters, conceived in order to monitor the System behavior in detail. The hostile working conditions of the experiment, especially due to the high radiation rate and dose absorbed during data taking, imposed to design a system which could be easily controllable and having a suitable set of diagnostic tools. The system structure is complex due to the fact that the shapes and kinds of detectors, and also the grouping of channels from the on-detector electronics to the off-detector one, vary considerably across it.

Figure 1: Muon System architecture

The front-end control hardware is based on the Service Boards (SB), designed around the ELMB, while the off detector electronics (ODE boards) integrate the ELMB on itself. Most of the monitor and configuration registers are integrated on two custom circuits: the DIALOG chip [2] on the front-end boards and the SYNC chip [3] on the ODE boards.

The LHCb Experiment Control System (ECS) software, and its part concerning the Muon System as well, is based on a PVSSII framework.

II. MUON ELECTRONICS
The DAQ electronics can be resumed on three main building blocks: the detector readout, the Service Board system and the ODE boards.
A. Detector Readout

The LHCb Muon Detector consists of about 120 thousands physical channels whose signals will be processed by the front-end readout system, resulting in 26,000 logical channels used for triggering purposes and offline muon identification. Each physical channel will be read by a single Amplifier-Shaper-Discriminator (ASD) circuit. A single FE board consists of two 8-channel ASICs called CARIOCA [2] and one mainly digital ASIC called DIALOG [3], both have been implemented in an IBM 0.25um radiation-hard CMOS process. In front of each channel connected to the chamber (strip or pad) there are spark protection components.

B. Detector Readout Control System

The Embedded Local Monitor Board [7] (ELMB) is the core of the ECS system. It is in charge of accessing and controlling all Service Board, Pulse Distribution Module and front-end components. As a consequence of the ELMB centre role, many multi-device procedures can also be written inside its firmware, therefore reducing execution time and CPU load otherwise increased by running such procedures on the main control computers. This approach shows a substantial degree of parallelism, which is reflected into about 600 ELMB microcontrollers utilized in the apparatus.

Another key component is the Timing, Trigger and Control [5] receiver (TTCrx). The TTCrx chip recovers and distributes the 40.08 MHz LHC clock machine with minimum jitter via an optical fiber link. The LHC clock signal arrives to the TTCrx and is recovered by means of two independent high-resolution phase shifters, providing a programmable delay, afterwards available for synchronization purposes. In addition it contains bunch-crossing and event counters. The former counts the number of bunch-crossings while the latter the events accepted by L0 trigger. TTCrx can also receive broadcast or individually-addressed commands from the TTC distribution network (each TTCrx into the LHC clock distribution system has a unique 14-bit channel identification number). TTCrx is also in charge of transmitting first-level trigger accepted decisions and their associated bunch and event identification numbers.

C. The Pulse Distribution Board

The Pulse Distribution Board [5] (see Figure 2) has been implemented mainly to distribute the machine clock (from the TTCrx chip) to Service Boards and to generate pulses (by means of logic implemented in an FPGA) at set bunch-crossing identification numbers, based on the TTCrx bunch-crossing counter, or at specific Timing and Fast Control [6] (TFC) commands to the Service Boards. Communication is controlled by the on-board ELMB. Both components, TTCrx and FPGA, are accessible via I^2C protocol. The PDM has additional components to reset and power cycle all other ELMBs in each ECS crate.

D. The Service Board

The Service Board [6] (see Figure 3) has been implemented to adapt ELMB for FEE control. A Service Board can host up to 4 ELMBs. Many additional features have been included in the board: 12 ports for front-end electronics control, 4 flash SPI and one EEPROM memory devices, 32 input/output digital signals and an FPGA used mainly to generate synchronous pulses for the front-end electronics.

E. The Off Detector Electronics Board

The Off Detector Electronics (ODE) [4] board is the Level-0 (L0) stage of the LHCb Muon detector. Each board receives 192 digital inputs from the detector front end electronics at 40 MHz rate and provides L0 trigger and DAQ interfaces. 24 custom chips (SYNC, receive the incoming signals and implement bunch crossing synchronization, time measurements, fine time histograms and L0 pipelines. A board controller (L0 controller), developed in a flash-RAM based FPGA, manages the trigger interface via 12 channels parallel optical link and the DAQ interface via single optical link working at 1.6 Gbit/s each. A TTCrx chip is used to receive the LHCb master clock and the control signals. An CAN-bus based interface is used to communicate with the experimental control system (ECS). A total of 152 ODE boards are used in the Muon System.
III. ECS Full System Outline

ECS electronic boards are inserted into 10 equipment Racks, alongside the Muon Detector. A Rack consists mainly of one Service Board System (one PDM and up to 20 SBs) one crate of ODE boards (up to 20 ODEs). A custom back-plane is used to distribute timing signals between the boards in the Service Board Crate instead any ODE board receive its TTC signals directly from the LHCb Timing and Fast Control TFC. Each Service Board crate is connected to a different detector sector. The whole system is controlled by six computers for the Service Board system (Figure 4), four computer for the ODE System and two computers to manage the hierarchy.

| 120,000 readout channels | 600 microcontrollers on 10 crates | 6 PCs |

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Figure 4: Overview of the Service Board control system

IV. Monitoring and Test Procedures

A. Detector Monitoring

1) Threshold Scan (Offset and ENC measurement)

2) Noise Rate

B. ODE

1) Time Histogram

C. Detector Readout & ODE Procedures

1) Connectivity

2) Timing Alignment

V. DAQ FSM

The whole system is controlled by a Finite State Machine through a strictly hierarchical structure (Figure 5), which moves across the system architecture. The basic element of the structure is the Hardware Unit and the corresponding Control and Device Units. A single Hardware Unit comprises one single ODE board (192 channels) and all the front-end electronics channels connected to it on detector (336 to 2304 channels). This results in having one ODE Device Unit and as many Device Units as the number of chambers connected to it (one Device Unit per chamber).

The main components of the DAQ FSM hierarchy are the Device Units: Chamber, ODE, SB-ELMB and PDM. Those are units where the states and commands are defined according to the detector and electronics parameters. The Control Units should practically replicate and carry the DUs states and commands up and down through the hierarchy.

The organization of the data points inside the Chamber and ODE Device Units have been realized with special care, due to the large number of registers to be handled (order 1000 per Device Unit). The communication between the OPC servers and the hardware registers is also a critical issue. Whenever possible, it has been optimized and parallelized by a suitable design of the ELMB firmware [8].

Figure 5: FSM hierarchy of the Muon ECS

A. Detector Readout and its Control System

In the ECS system, about 122000 FE channels, roughly 700000 control registers, will be managed by a PVSS based software running in a distributed mode on six computers. In addition many user-friendly panels have been developed. Many of them are shown in Figure 7.

A FSM hierarchy for the chambers and control electronics structure has been designed by means of well defined commands and rules in order to describe state transition conditions and automatic reactions according to detector and electronics parameters variations. Figure 6 shows a scheme of the ECS FSM hierarchy and its main possible states.

Figure 6: FSM hierarchy scheme for detector readout supervise

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PVSS and FSM structures can be built from a custom made script based on a mapping file describing all the connections from the devices to be monitored up to the high level control components. It makes the system very flexible; the whole system can be reconfigured in few minutes.

Figure 7: Main control panels for the LHCb Muon Chambers and their Control Electronics

VI. CONCLUSIONS

The ECS System is now under commissioning in the LHCb apparatus. The system is now mainly used to debug the connectivity of the apparatus and to performs time alignment using PDM pulse system.

REFERENCES

[8] V. Bocci et al. ELMB Microcontroller Firmware and SCADA Integration for the LHCb Muon Detector Readout