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Differential, voltage sensitive preamplifiers for bolometric detectors

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Abstract

We present two differential voltage sensitive preamplifiers to read-out very slow and fast cryogenic detectors. The first one operates at room temperature, while the second one, made in a monolithic GaAs MESFET process, is optimized for 4.2 K.

1. Introduction

To reduce disturbances originating in long interconnecting links, cryogenic detectors must be read out with low noise preamplifiers, located in the detector's vicinities. The preamplifiers, therefore, should be able to work at very low temperatures. This condition can be easily satisfied when one or just a few channels are required by the experiment. In the case of a detector array using many channels the mentioned condition is more difficult to satisfy. The power dissipation and the space occupation are very critical parameters to account for, especially when the refrigerator system must reach the lowest possible temperature. The room temperature preamplifier to be described in this paper has been designed to read out an array of presently four, but in the near future at least twenty, large mass (330 g each) TeO_2 bolometric detectors.

The signal generated in these detectors is very slow, its frequency spectrum being confined in a few tens of Hz. As a consequence, the electrical capacitance shunting the detector may not limit the energy resolution of the system, even when the thermistor impedance is quite large, of the order of a few hundred MΩ. This circumstance can be exploited in two ways. Firstly the preamplifier can be located relatively far from the detector, outside the refrigerating system. Secondly, the preamplifier's input device can be made of large gate area, with no restriction in power dissipation, reducing its series noise contribution.

Microphonic noise, increasing with the length of the link, may be worst if the preamplifier is located outside the refrigerator. The effects of this noise can be attenuated if a symmetrical connection between the detector and the preamplifier is used, and a Differential Voltage Preamplifier (DVP) is adopted for the read-out. This was the choice for the realization of the present read-out of the array of TeO_2 detectors which is working at the Gran Sasso Underground Laboratory [1].

In addition we have also developed cryogenic preamplifiers able to work down to 1 K for applications with faster detectors. The preamplifiers were realized, using a monolithic GaAs MESFET technology. Each chip contains a DVP which, if needed, can be separated into two single ended voltage preamplifiers, by using an additional pin connection. Low noise and power dissipation where considered in the design.

In the following sections the room temperature and the low temperature DVP will be illustrated.

2. Room temperature differential voltage preamplifier

A DVP suitable for bolometer read-out must satisfy two conditions. The first one is to have a very large input impedance. The second one is to have a low noise. Earlier we have developed a configuration which permitted to meet those two conditions: a very large input impedance, like the one obtained with the instrumentation amplifiers, but using only one pair of JFET transistors at the input, saving a factor $\sqrt{2}$ in the noise [2]. This previous version of the DVP has been simplified and the circuit has now a new feature: to be fully DC coupled to the detector, allowing the measurement of detector temperature drifts.

The schematic circuit is shown in Fig. 1. The input transistors Q_1 and Q_2 are interconnected trough resistors R_A. The feedback loop is realized by means of resistors R_A and R_B. The closed loop gain is given by $R_B/R_A + 1$. To obtain high open loop gain the differential input common source stage (Q_1 and Q_2), loaded by the two resistors R_1 and R_2, is converted to a single ended output and amplified by a standard operational amplifier (OA) (LF356). The network is compensated with the capacitance C_C. The two current generators I_{B1} and I_{B2} permit to compensate the output DC offset voltage.

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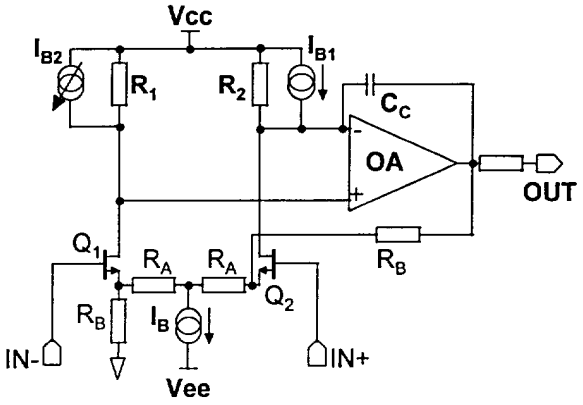

Fig. 1. Circuit schematic of the room temperature differential voltage sensitive preamplifier.

This preamplifier was implemented as a first stage of a processing chain which consisted also of an additional gain stage and an active four pole low pass filter (Bessel filter). All the three parts were made programmable: the gain of both the preamplifier and the additional gain stage can be varied and the cutoff frequency of the Bessel filter can be easily changed. The maximum differential voltage gain of the preamplifier was fixed to 218. With this gain the frequency bandwidth was limited to about 20 kHz. The maximum output signal swing is ± 10 V. The integral non-linearity in this range is 0.5%, which reduces to 0.05% in the ± 8.5 V range (± 39 mV maximum input signal). This result was obtained thanks to the large open loop gain of the circuit. The differential input impedance resulted in about 30 pF. The Common Mode Rejection Ratio, CMRR, is 110 dB from DC to about 350 Hz, remaining greater than 85 dB up to5 KHz. The series noise is low thanks to the input JFETs Toshiba 2SK146. The series white noise is about 3 nV/$\sqrt{\text{Hz}}$, limited by the R_A resistors (360 Ω total), which serve to maintain low the output voltage drift. At 1 Hz the measured noise is 20 nV/$\sqrt{\text{Hz}}$, it depends on $1/f^{\alpha}$ with α equal to about 0.7. At 0.1 Hz we measured 100 nV/$\sqrt{\text{Hz}}$, with an evident presence of a Lorentzian [3], with some hundreds of mHz corner frequency. The shot noise due to the gate leakage current of the input JFETs, less than 2 pA, was responsible for the parallel noise. We are planning to reduce this noise by lowering the temperature of the input JFETs to about -50°C by using Peltier cells.

3. Cryogenic differential and single-ended voltage preamplifier

This cryogenic DVP was designed with the aim to obtain low noise and low power dissipation. We have used a monolithic process which gives the advantage of design flexibility and small circuit size. This feature is particularly useful as the space inside a refrigerator system if often limited. To be able to work down to very low temperature, 4.2 K or less, the choice was for the GaAs MESFET technology [4]. A first version of this preamplifier [5] was realized with a configuration similar to the room temperature DVP described in Section 2. Now a new version has been implemented with new features included. In the first preamplifier version a contribution to the input series noise coming from the second stage was present. The area and the bias conditions of the components in the second stage are now realized with proper dimensions, to minimize their noise contribution. Their expected effect in noise level should be now limited to less than 15–20%. The open loop gain has been incremented to improve the integral linearity further. By introducing only one additional pin, the circuit can now operate even as a dual channel single ended voltage preamplifier.

Dynamic tests have shown very good results at both 4.2 and 77 K. The differential gain was fixed to 11. The resulting frequency bandwidth was about 3 MHz. The power dissipation was limited to 13 mW ($V_{CC} = 2.5$ V and $V_{EE} = -1$ V). Input impedance resulted in less than 10 pF. The measured CMRR was 75 dB up to more than 1 kHz, and the integral non-linearity was only 0.03% in the ± 120 mV output swing (± 11 mV maximum input signal). Parallel noise was completely negligible thanks to the vanishing gate leakage current at low temperature. The low frequency series noise was this time limited by the process to about 100 nV/$\sqrt{\text{Hz}}$ at 100 Hz, with a $1/\sqrt{f}$ roll off, at both 77 and 4.2 K, coinciding with the series noise of each input transistor, which has a dimension ($L \times W$) of 3×6000 μm^2. The noise expected was about 15 nV/$\sqrt{\text{Hz}}$ at 100 Hz. The present process run, although within the characteristics warranted by the foundary, was at the lower limit in the doping level. This fact determined poor noise performance at cryogenic temperatures. A new process run is foreseen to solve this.

4. Conclusions

Two Differential Voltage sensitive Preamplifiers (DVP) for bolometric detectors have been realized following different strategies. A room temperature DVP able to read-out the very slow signals coming from arrays of large mass bolometric detectors feature low noise and high linearity. A cryogenic monolithic GaAs DVP able to work from 1 K up to at least 77 K to read-out faster detectors showed very good dynamic performance at low power dissipation. The cryogenic DVP is even able to work as a dual channel single ended preamplifier by proper connection of a programming pin.

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