The Programmable Front-End System for CUORICINO, An Array of Large-Mass Bolometers

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***Abstract*—We report on the front-end electronics designed for the readout of the CUORICINO experiment's array of 60 large-mass bolometers. The front end consists of a preamplifier and a bias system for the bolometer. A significant feature of our design is its capability for *in situ* DC characterization of each bolometer as a function of applied bias. The principal front-end operating parameters, low-noise bias selection, load resistor selection, offset compensation, and gain are remotely programmable.**

***Index Terms*—Detector biasing, electronics for bolometric detectors, front-end readout, high-input impedance circuit, low noise, low noise amplifier, low thermal drift, programmable system.**

I. Introduction

In the case of experiments that implement an array of many detectors, accommodating the dynamic range of the detectors, demands flexibility and partial or full remote programmability in the front-end electronics [1], [2]. Bolometers, for which the manufacturing spread of dynamic characteristics is particularly broad, are especially demanding in this regard [3]. In addition a further requirement to the readout is for very low series and parallel noise at low frequency, for both the amplification system and the bias network. Finally, a last important requirement is that the front-end drift must be negligible to allow continuous monitoring of the detector baseline.

The CUORICINO [4] experiment plans to measure an array of 60 large-mass bolometric detectors for a time exceeding two years. To limit the manual interventions in the vicinity of the bolometers during the observing period, that can interfere the measurement, we have implemented a front-end system that enables remote adjustment of the principal operating parameters, detector by detector. We begin in the next section with a system-level overview and follow in subsequent sections with descriptions of the various subsystems.

II. System Description

Among the demanding constraints imposed on the CUORICINO front-end system is the restricted space into which the hardware must fit. The space available is the space now occupied by the front end [5] of the predecessor experiment MIBETA [6], an array of only 20 channels. We were thus obliged to increase the channel density by a factor of four, and we achieved this compaction while retaining standard 19 in card cages (19 in $\times$ 4 in $\times$ 10 in) as the housing for the modules. Each card cage accommodates 15 *Main Boards* (MB). Each MB is 100 mm $\times$ 220 mm and comprises two complete analog channels and their associated logic circuitry. Also a very stable low-noise voltage supply/reference [7], is accommodated in every cage to service all the cards there present.

In Fig. 1, we show the functional block diagram of one of the two channels on an MB. Each channel has its own digital logic section, which sets the controls for the associated analog section. The control signals customize the analog section for the detector element that it serves. We implemented the logic section as a daughter card of the MB. The preamplifier portion of the analog section and the load resistor system are also on daughter cards.

A single input connector at the rear of the MB serves both channels. A single 37-pin "D" connector at the front accommodates the 12-lines differential analog output bus, a 10-line bidirectional digital bus, power at $\pm$12 V and 5 V, the $\pm$10 V supply/reference voltages, and the detector bias voltage as well as ground.

We laid out the channels symmetrically with respect to the midline of the card, and we took care in the layout to minimize crosstalk. For example the power and ground conductors are split at the midline of the module and join only at a mecca near the output connector. We measured the crosstalk from one channel to its neighbor on the MB to be at the level of $-$120 dB.

III. Load Resistor System

To each element of the bolometer array is attached a Neutron Transmutation Doped (NTD) thermistor, which converts the thermal signal to a voltage signal. The bias current for the thermistor is sourced through a pair of low-noise large value thick-film 27 GΩ resistors as shown in Fig. 2. These resistors are manufactured by Siegert. They have been selected for their low $1/f$ noise when biased at the current levels required by the detectors [8]. V_{b1} and V_{b2} are the voltages delivered by the programmable bias attenuator described in the next section.

We represent the thermistor with a dashed line to indicate that it is within the cryostat. All other components of this circuit are at ambient temperature. We connect the cold thermistor to the warm front end with shielded twisted pair. The common mode rejection of this symmetric differential configuration effectively

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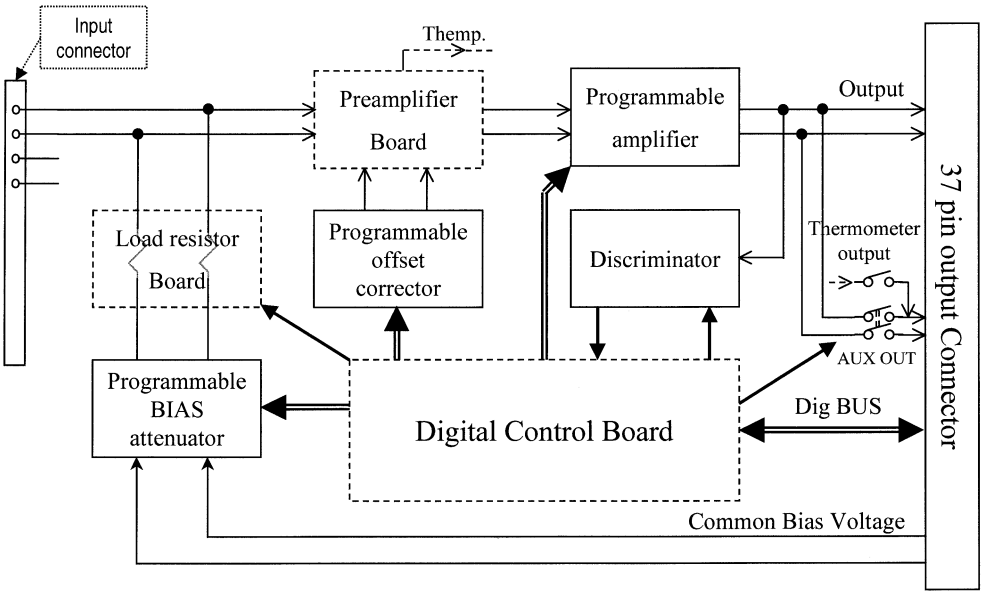

Fig. 1. Schematic of one channel of the two present on each CUORICINO main board (MB).

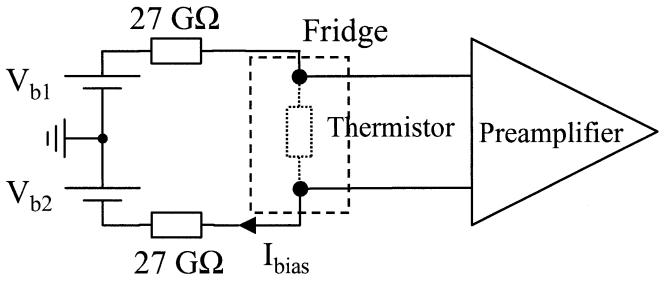

Fig. 2. Schematic of the thermistor biasing system.

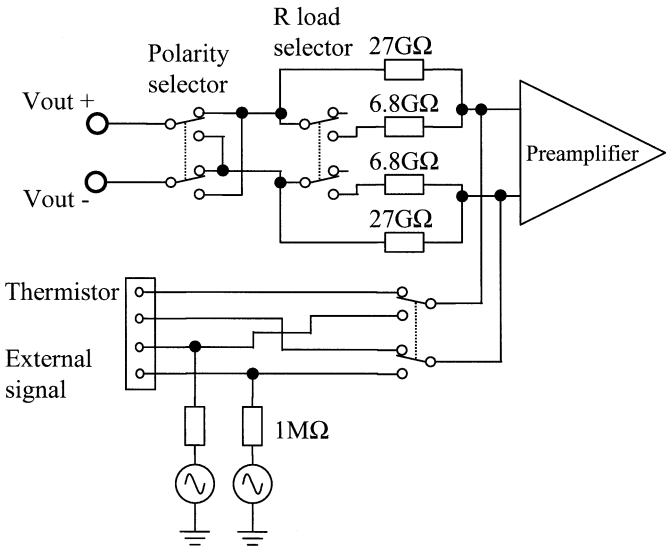

Fig. 3. Configuration options at the preamplifier input.

suppresses adjacent-channel crosstalk and microphonic noise induced by wire vibration.

The load resistor daughter card also accommodates a pair of 6.8 GΩ resistors in surface-mount packages. By means of a bistable relay on the MB and shown in Fig. 3 we can programmably connect the 6.8 GΩ resistors in parallel with the 27 GΩ resistors for the purpose of *in situ* current-voltage, *I-V*, characterization of the thermistor. Because the relay need be energized only briefly to set its state, thanks to its memory, during normal operation it does not consume power and his coil does not create electromagnetic interference.

As shown in Fig. 3, an additional bistable relay can disconnect the preamplifier inputs from the thermistor and reconnect them to a test signal source. A test signal may be generated on the MB and inserted through the 1 MΩ resistors, or an externally generated signal may be applied directly to the preamplifier input. In the test configuration it is also possible to measure the current in the load resistors.

We adopted a number of methods in the layout to suppress parasitic conductance that might compromise the high impedance of the input nodes. First, we segregated the inverting and noninverting inputs by layer, consigning one to inner layer 1 and the other to inner layer 2. Second, we placed guard traces on the top and bottom layers paralleling the respective signal traces on inner layers 1 and 2. Third, we maintained a minimum separation of 200 mil (5.08 mm) between high-impedance pins, even at the pins of the relays. The spacing of the pins was an important consideration in the selection of the NAIS DS2ESL2-12 V for the bistable relay. Fourth, as shown in the photograph of Fig. 4, we created arc-shaped apertures in the circuit board substrate adjacent to each relay pin as a barrier to solder flux. Solder residues that elude the post-assembly wash would be problematic, but the apertures nearly eliminate the contribution of such residues to parasitic conductance. With these layout precautions and conventional industrial assembly procedures we obtain excellent results.

IV. Programmable Bias Attenuator

The inherent large spread in bolometer optimum operating point, between 100 pA and 300 pA, requires that the bias current of a channel be individually adjusted. In addition, the *I-V*

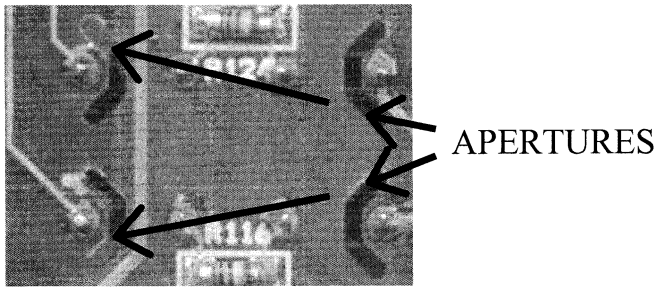

Fig. 4. Photograph of a portion of the printed circuit board showing the apertures that suppress parasitic conductance at the relay pins.

bolometer characteristics are explored over a larger range, up to about 4.5 nA or 60 V across the two smaller selectable load resistors, 6.8 GΩ+ 6.8 GΩ. For this reason, with each channel we include a programmable attenuator, which produces the bias voltage as an adjustable fraction of a common reference voltage. For the reference voltage source we use a single Agilent Technologies 6627A system power supply, which offers the required precision and stability.

In Fig. 5, we show the schematic of the attenuator. This circuit is an adaptation of an R-2R ladder network. The mean value of the reference inputs, $(V_+ + V_-)/2$, establishes the ground of the thermistor circuit. Then, with respect to this ground

$$V_{\mathrm{OUT}+} = -V_{\mathrm{OUT}-} = \frac{n}{64}\,(V_+ - V_-) \tag{1}$$

where n is the value of five bits of input latched in the digital section of the channel.

In the usual implementation of an R-2R ladder the upstream leads of the 2R resistors are shunted either to the reference voltage or to ground. We implement only the most significant bit, Bit_4, in this manner using a bistable *Double-Pole Double-Throw* (DPDT) relay, for obtaining maximum accuracy. For the other four bits we adopted a less precise but space-saving strategy. The 2R resistors are permanently connected to the reference voltages through pull-up resistors R_p small compared to R. For the value of R_p we selected R/6. The corresponding R_p-2R junctions on the positive and negative sides of the ladder are bridged by a photo-MOS switch controlled by one of the digital input bits. When the switch is open, the R_p-2R chain increases the output voltage by an amount proportional to its position in the ladder. With the switch closed and tying the opposing R_p-2R junctions into a single node, we see that these nodes, being symmetrically placed between the positive and negative sides of the ladder, will be at ground potential as required. The use of the resistors R_p in lieu of switches is an approximation of the ideal ladder design, but it saves the scarce space that eight additional photo-MOS switches would occupy.

The 2R and R resistors in our attenuator are 560 kΩ and 270 kΩ, a ratio higher than 2:1. When the photo-MOS switch is open, the effective value of the 2R resistor is still higher, $2R+R_p$. The maximum calculated deviation of this circuit from an ideal R-2R ladder is -5%. Measured integral nonlinearity and differential linearity with respect to each calculated setting of the implemented network of Fig. 5 was about 0.3% and 3.2%, respectively.

For the filter capacitors C_1 and C_2, 33 μF and 10 μF respectively, we selected parts that stand off a considerable voltage regardless of polarity. The photo-MOS switches, IR PVT 322, also stand off a considerable voltage enabling the attenuator as a whole to withstand the application of $|V_+ - V_-| = 60$ V at its inputs.

Between the attenuator outputs and the 27 GΩ load resistors we have interposed a bistable DPDT relay shown in Fig. 3. This relay allows us to invert the polarity of the bias voltage, and by this means we can account for the thermocouple effect operating in the wires that connect the front end to the thermistor.

The noise measured between the output nodes $V_{\mathrm{OUT}+}$ and $V_{\mathrm{OUT}-}$ of Fig. 5 is 28 nV/$\sqrt{\mathrm{Hz}}$ at 1 Hz, see Fig. 6, which is negligible compared with 20 μV/$\sqrt{\mathrm{Hz}}$, the series thermal noise of the 27 GΩ resistors.

V. The Preamplifier

As a preliminary we offer a general discussion of four issues that substantially influence the design of the preamplifier. First, the dynamic impedance of a semiconductor bolometer is the sum of a real and a positive imaginary part [9]. For this source impedance and signals such as nuclear decays induced in the bolometer, a voltage amplifier is the conventional approach. Its performance is not superior to a current or charge configuration [10], but it allows its inputs to float. This feature makes biasing of the bolometer compatible with DC coupling.

Second, the distance from the bolometer to the front end make the input sensitive to microphonically induced noise. Our bolometers operate in the range of 10 to 100 mK whereas the first stage of the front end can operate at temperatures from a few Kelvins [11] up to room temperature. The distance separating the two thermal regimes can be no less than a few tens of centimeters and may more conveniently be a few meters. The long leads that transport the signal across the thermal gap are antennas for microphonic noise. We address this issue by making the preamplifier input differential. The amplifier noise in differential configuration is twice, in power, compared with the single-ended input, but in this case, we achieve efficient suppression of the more troublesome microphonic noise, which is predominantly common mode.

Third, for our large-mass bolometers the signal bandwidth extends from roughly 1 Hz to a few tens of Hertz. Thus, the amplifier noise, both series and parallel, must be minimized at low frequency. Finally, we must be able to monitor the baseline of each bolometer and to correlate shifts in the baseline with the bolometer's energy gain. This capability demands adequately low thermal drift in the preamplifier.

Considering the above issues we designed and implemented the circuit shown in Fig. 7. The circuit operates at room temperature. At the core of the design is the JFET pair J_1 and J_2, which accepts the differential input. The series *Low-Frequency* (LF) noise is a major consideration in the selection of these transistors. The current source G_1 [12] biases each JFET with a current of about 1 mA. We minimize parallel noise by establishing V_{DS} at about 0.8 V, the lowest value consistent with adequate gain. The op-amps A_1 and A_2, connected in the cascode configuration with J_1 and J_2, fix the V_{DS} for both JFETs to be the same as the

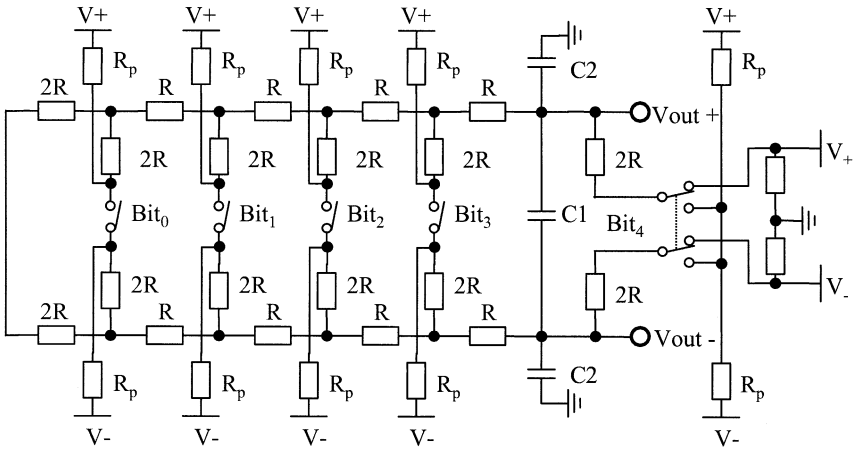

Fig. 5. Schematic of the programmable bias attenuator.

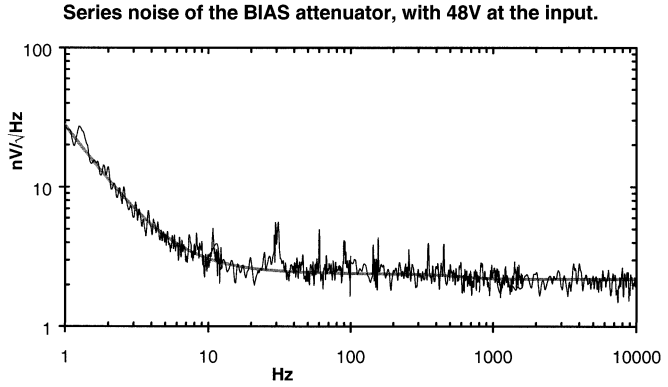

Fig. 6. Output noise of the BIAS attenuator system.

voltage at the top of R_G. Then $V_{\rm DS} = I_2 R_G - (I_1 - I_2)R_S/2$ where I_1 and I_2 are the currents of the current sources G_1 and G_2.

The connection of the outputs of op-amps A_3 and A_4 through the resistors R_F to the sources of J_1 and J_2 closes the feedback loop. The feedback establishes the gain at $(R_F + R_S)/R_S$, with $R_F = 20\ \text{k}\Omega$ and $R_S = 91\ \Omega$ the gain is 220 V/V. The sources of J_1 and J_2 are directly accessible at the connectors OFF Adj + and OFF Adj – for the purpose of trimming the offset voltage. The values of capacitors C_1, C_2, and C_3, used for frequency compensation, are dependant on the op-amps adopted. The inverter A_5 enables a differential output.

Neither the input JFETs nor any of the op-amp circuits are individually compensated for ambient temperature drift. We deal with this issue by trimming the circuit as a whole. First, we operate the preamplifier in a temperature-controlled chamber to determine the untrimmed thermal response. Then, we inject at the virtual ground node labeled THERM in Fig. 7, a current proportional to temperature that will cancel the measured drift. We generate the compensating current using the circuit shown in Fig. 8. The base-collector junction of one or the other of the two transistors is the thermometer. The op-amp buffers the voltage developed across this junction, and the network R_A-R_B approximately reverses the junction drop thereby allowing the op-amp output to be zero at a temperature T_0 in the vicinity of 20 °C. The resistor $R_{\rm TH}$, working between the op-amp output and a virtual ground, converts the junction voltage to a current $\Delta I = (\pm 2\ \text{mV/°C})(T - T_0)/R_{\rm TH}$. We trim $R_{\rm TH}$ and set the switches S_1 and S_2 so that this current just cancels the uncompensated drift of the individual preamplifier as we measured it. The switches determine which of the two junctions is active and thus the sign of $\Delta I/\Delta T$. With this technique we are able to reduce an uncompensated drift as large as 60 μV/°C to about 0.1 μV/°C.

The diode used in the temperature compensation circuit should exhibit low noise, and we measured the noise of many transistors and diodes in search of a suitable device. We determined that the pnp transistor BC858 is adequate for our purpose. At a bias current of 100 μA its LF noise is between 20 and 30 nV/$\sqrt{\text{Hz}}$ at 1 Hz, with a $1/\sqrt{f}$ slope. Taking $V_{\rm IDRIFT}$ to be the thermal drift of the preamplifier referenced to the preamplifier input, $V_{\rm DDRIFT}$ to be the temperature coefficient of the BC858 junction, roughly -2 mV/°C, A to be the voltage gain, 220 V/V, and $\alpha \approx R_1/R_{\rm TH}$, where R_1 is from Fig. 7 and $R_A \gg R_B$ in Fig. 8, we see that we achieve compensation provided that $\alpha V_{\rm DDRIFT} = A V_{\rm IDRIFT}$. With $\overline{e_{\rm DN}^2}$ representing the junction noise, the contribution of the temperature compensation circuit to the noise budget, referenced to the input is

$$\overline{e_{\rm DIN}^2} = \left(\frac{V_{\rm IDRIFT}}{V_{\rm DDRIFT}}\right)^2 \overline{e_{\rm DN}^2}. \tag{2}$$

For example, for a large initial drift of 60 μV/°C and 30 nV/$\sqrt{\text{Hz}}$ diode noise, temperature compensation will contribute 0.9 nV/$\sqrt{\text{Hz}}$ at 1 Hz, which is to be added in quadrature with the preamplifier noise.

The noise level of this preamplifier is quite suitable for the application. The gate current of each JFET is less than 0.3 pA, which corresponds to parallel noise of about 0.3 fA/$\sqrt{\text{Hz}}$. The series noise of the preamplifier, after temperature compensation, is shown in Fig. 9. The LF noise is about 4.6 nV/$\sqrt{\text{Hz}}$ at 1 Hz with a $1/\sqrt{f}$ slope. The white component, $\approx$ 2.5 nV/$\sqrt{\text{Hz}}$, arises in roughly equal parts from the JFETs and the thermal noise of the 91 Ω feedback resistors R_S. Making these resistors smaller would reduce the noise, but then the offset voltage trim currents (at the OFF Adj + and OFF Adj – nodes of Fig. 7) would become unacceptably high. Much of the offset voltage results

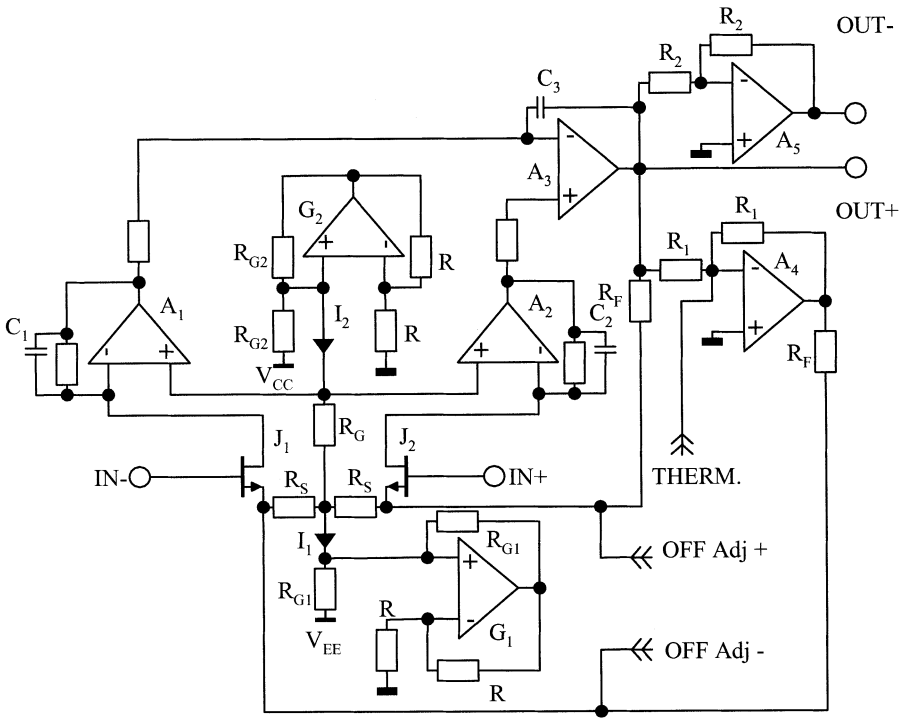

Fig. 7. Circuit diagram of the voltage sensitive preamplifier implemented.

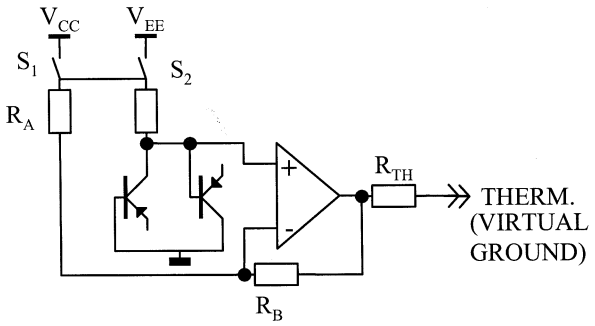

Fig. 8. Circuit diagram of the drift correcting circuit.

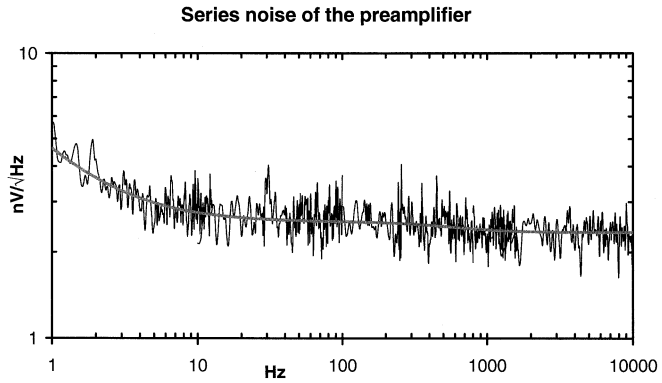

Fig. 9. Series noise of differential voltage sensitive preamplifier.

from the biasing of the DC coupled bolometer, and convenient offset trimming is thus an essential feature.

The preamplifier daughter card is a four-layer printed circuit board with dimensions of 55.9 mm × 38.1 mm. In addition to the circuitry discussed above this card accommodates an analog thermometer, LM50, which allows us to monitor the preamplifier temperature remotely.

VI. The Offset Corrector

Because the bolometer is DC coupled to the front end, the biasing contributes to the input offset voltage. In this situation a sophisticated system for offset trimming is more than a convenience. As low noise is a prerequisite in our application, the offset corrector and its reference source clearly must also conform to the low-noise criterion.

For the voltage reference we adopted a design that we described in an earlier report [7]. This solution avoids a local monolithic reference and its extremely low-pass filter, by implementing them in the unit that supply the circuit with the +10 and −10 V voltage. The reference voltages used in the offset corrector, −2.12 and +6.76 V, are derived locally from the system-wide references using resistive dividers.

The application of a differential current ΔI_{CURR} through the preamplifier connections OFF Adj + and OFF Adj – to the JFET source resistors R_S (see Fig. 7) will generate the offset compensating voltage V_{OFFSET}. Clearly

$$\Delta I_{\mathrm{CURR}} = \frac{V_{\mathrm{OFFSET}}}{R_S}. \tag{3}$$

The bolometer bias voltage is typically between 10 and 20 mV. For characterizing DC behavior, however, a bias voltage as high as 50 mV may be appropriate. The JFETs can contribute an additional ±20 mV to the offset budget. A range for V_{OFFSET} of ±80 mV is thus conservative, and with R_S set at 91 Ω (3) gives a corresponding range for ΔI_{CURR} of about 900 μA.

The correction current ΔI_{CURR} is the difference $I_{\mathrm{off}+} - I_{\mathrm{off}-}$ where these currents appear at the outputs of the pair of current sources shown in Fig. 10. The resistor chain R_2-R_3 sinks only 35 μA and allows both current sources to remain conducting regardless of the state of the switches. A current with the magnitude of ΔI_{CURR} flows from node A through one current source

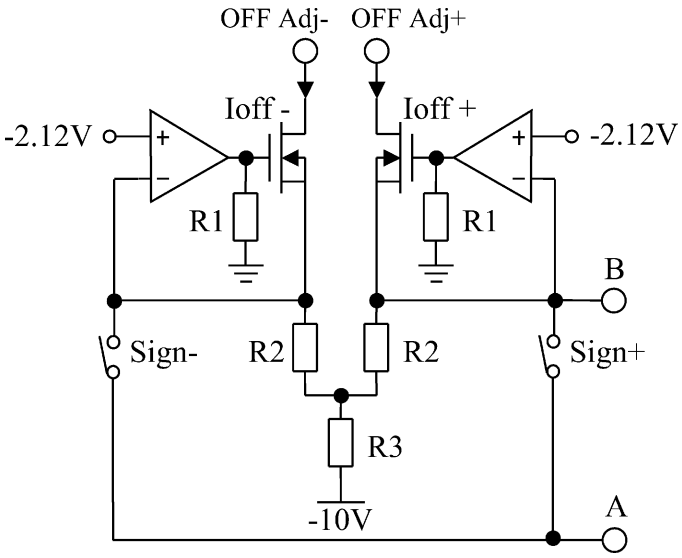

Fig. 10. Current generator setup for the offset correction.

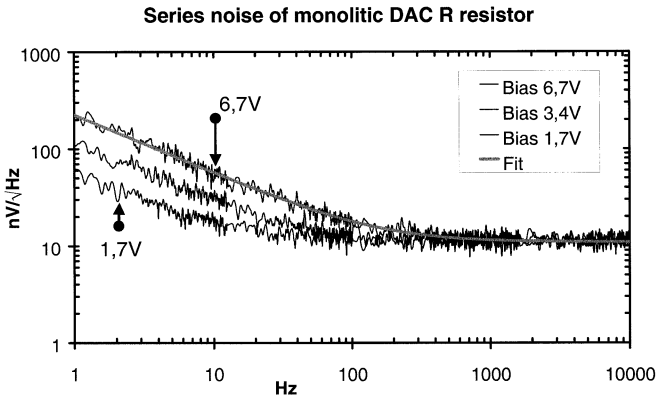

Fig. 11. Noise performance of the adopted DAC for three bias voltages.

or the other depending on which one of the switches Sign- and Sign+ is closed. For the switches we use the MAX4605, which is a MOS switch with a low ON resistance, $Ron = 5\ \Omega$. The resistors R_1, 1 kΩ, load the outputs of the op-amps and so improve their stability. The op-amps ensure that the MOSFET source voltage is the same as the reference, -2.12 V. The MOSFET drains are in common with the sources of the JFETs of the preamplifier circuit (Fig. 7), and these are generally at a positive potential because in normal operation the common-mode voltage appearing at the preamplifier inputs is close to 0 V.

Our objective is that the current inserted at node A of Fig. 10 should be programmable, and thus we need to incorporate a digital-to-analog converter, a DAC, into our design. A commercial DAC would be convenient, but generally the output buffer of these devices renders them excessively noisy for this application, particularly for DAC based on CMOS technology. The DAC that we adopted, the 12-bit DAC8043A, circumvents this problem by omitting the output buffer, but it is not enough for the noise performance needed. The DAC adopted operate by means of a current scaling R-2R network. Unfortunately resistors on integrated circuits exhibit LF noise proportional to the square of the applied voltage [13], [14]. Fig. 11 shows the noise from the DAC8043A with three choices of the reference voltage and confirms the last assertion. The noise from this DAC is tolerable provided the reference voltage is sufficiently low, but then

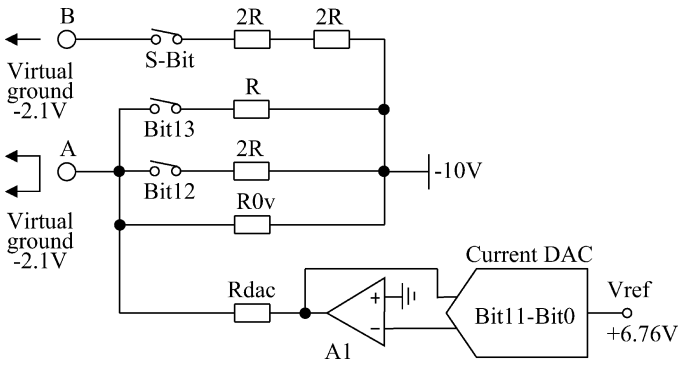

Fig. 12. Circuit for the generation of the programmable current.

the maximum current derivable from it is inadequate. Our solution was to cascade the DAC8043A with an external low-noise buffer amplifier, implementing a small precise and low noise trimming of the offset at the front-end output. The additional increase of the needed correction range has been obtained by injecting to the node A of Fig. 10 a correcting current provided by two low noise resistors, digitally controlled by switches. The DAC buffer can generate only a quarter of the maximum correcting current, the remaining being given by the two digitally selectable resistors.

Fig. 12 shows this solution. The metal-film resistors R and 2R, which set the supplemental current, introduce negligible LF noise. With value 18 kΩ, R enables the movement of V_{OFFSET} by 40 mV, and 2R enables an additional 20 mV. With V_{REF} at 6.76 V the DAC8043A contribution to the noise is only 0.9 nV/$\sqrt{}$Hz at 1 Hz referred to the preamplifier input. Working through R_{DAC}, 30 kΩ, the DAC8043A can move V_{OFFSET} by 20 mV, bringing the total excursion available to the desired 80 mV.

The resistor R_{0V}, 120 kΩ, sinks the current that would otherwise flow through R_{DAC} into A even when the DAC8043A output is at 0 V. Because resistors R and 2R have a precision of 1%, some narrow gaps may exist in the accessible range for V_{OFFSET}. These gaps have been partially taken into account by the addition of overlapping codes within the DAC range. The op-amp A_1, an LT1881, contributes to the noise at the level of 0.55 nV/$\sqrt{}$Hz at 1 Hz. The noise from the -10 V reference is about 95 nV/$\sqrt{}$Hz at 1 Hz and in the worst case may contribute 0.94 nV/$\sqrt{}$Hz at 1 Hz referred to the preamplifier input.

In Fig. 13 we show our measurement of front-end noise when the maximum offset compensation current is injected into the preamplifier. Comparing Fig. 13 with Fig. 9, we conclude that the increment of the compensation circuit to the noise of the preamplifier alone is at worst 4% at 1 Hz and becomes negligible at higher frequencies.

Under the control of the digital section a channel may autonomously trim its offset using a successive approximation method. Initiation of this process is by command delivered on the digital bus or by activation of a button on the MB front panel. The digital board determines the state of the bit under test by reading the output of the discriminator shown in Fig. 1. The comparator has a threshold of 114 mV and a hysteresis of 32 mV. The algorithm requires one cycle to set the polarity switches (Fig. 10) as well as a cycle for each of the 14 magnitude bits.

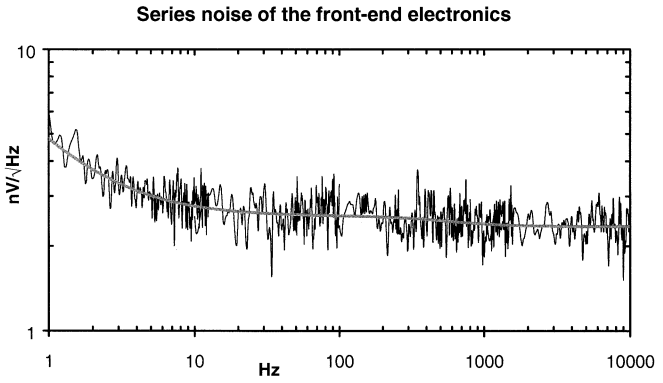

Fig. 13. Series noise of the front-end electronics when operated with the maximum current injected from the offset corrector.

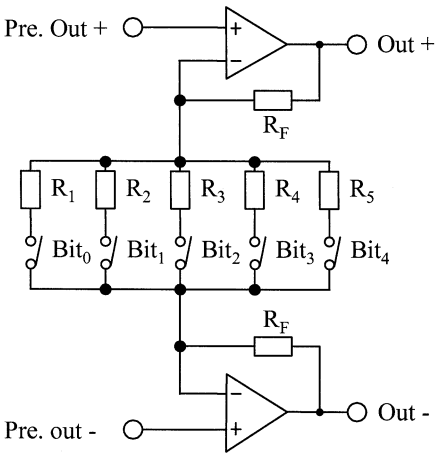

Fig. 14. The programmable gain amplifier.

Allowing this algorithm to run too fast may have two adverse consequences. First, inadequate settling times may introduce errors. Second, the system, acting like a unity-gain feedback loop, may break into oscillation. Slowing down the process solves both problems. The offset corrector algorithm operate with a reduced clock obtained from the output of a programmable counter.

After a channel has trimmed its offset, the resulting value of the DAC code is available via the bidirectional digital bus. Any value of offset may then be established by suitably adjusting this code and sending the new code to the channel. The Special bit, S-bit, shown in Fig. 12, facilitates such manipulations of the offset voltage. The current that it controls corresponds to roughly half of the range of the DAC8043A. If the code corresponding to null offset is in the lowermost quarter or the uppermost quarter of the DAC8043A range, then setting the S-bit and retrimming will shift the code for null offset to a value in the middle half of the range. For one setting of the S-bit or the other an excursion of the offset voltage by at least a quarter the range in both directions is possible without alteration to the less precise high-order bits 12 and 13. A quarter of the DAC8043A range corresponds to 5 mV at the input and a minimum of 1.1 V at the output. This range of correction is largely able to comply with the dynamic range required by the application.

VII. The Programmable Amplifier and System Noise Performance

The final stage of the signal processing chain is the programmable gain amplifier, which we show in Fig. 14. The circuit provides a digitally selectable choice of 32 values of gain in the range from 220 to 5000 V/V from preamplifier input to module output. Both input and output are differential. In this circuit we use metal-film resistors, MAX4605 switches, and AD822 op-amps. These components all have adequate LF noise behavior.

Because bolometers spread their characteristics over a large range, it is difficult to estimate the noise figure of the implemented readout. We try to do this considering the mean energy resolution of 3.1 keV_{FWHM} obtained from MIBETA experiment [4], with the best performance of the array close to 1.8 keV_{FWHM}. This performance is expected to be maintained also for CUORICINO [15], that foreseen bolometers with a mass as twice as those of MIBETA. The above mean resolution is obtained when the bolometer dynamic impedance is about 20 MΩ, the noise is about 0.82 $\mu\text{V}_{\text{FWHM}}$, and the frequency bandwidth of the signal is about 10 Hz [4]. The noise of the whole analog system, both series (about 6 $\text{nV}/\sqrt{\text{Hz}}$ at 1 Hz, $1/f$ slope) and parallel (about 0.4 $\text{fA}/\sqrt{\text{Hz}}$), results in about 37 nV_{FWHM}. The parallel thermal noise of the 2×27 GΩ load resistors is 82 nV_{FWHM}. Load resistors $1/f$ noise is negligible at the typical bolometer bias level of about 150 pA [4]. The total contribution results in about 90 nV_{FWHM}, dominated by the load resistors. This is considerable smaller than the noise quoted above, even for the better bolometers of MIBETA, proving that the designed front-end is adequate for this experiment.

VIII. The Digital Control Board

The *Digital Control Board* (DCB), communicates via a 10-bit bidirectional bus [6] with a personal computer. The low-order eight bits carry the data, and the high-order two bits carry the instruction code. Each channel in the system has a unique address, and the computer communicates with one channel at a time. The rudimentary protocol proceeds through four steps: addressing the channel, sending the command, transferring the data, and closing the transaction.

An *RC* oscillator built around an NE555 timer chip furnishes a 3.9 kHz clock to the DCB. The comparatively low frequency allows error-free communication even if the bus must be rather long. Because electrical noise originating from the clock is undesirable during data acquisition, the DCB can shut down the oscillator and normally allows the clock to run only when needed.

Each channel includes one *Complex Programmable Logic Device* (CPLD) for the implementation of the DCB functions. In addition the two channels on a MB share a third CPLD, which manages the communication. All three CPLDs are the Xilinx XCR3128XL. An uncommon feature of this device is that its outputs can remain active even when the clock is idle. A second feature that suits the XCR3128XL to our application is the low current consumption, only a few microamps at the operating frequency.

Signals exchanged between any channel and the computer pass through digital opto-couplers, which facilitates isolation of

the front-end ground from the computer ground. This isolation helps to protect the front end from disturbances in the computer ground.

IX. Conclusion

We have designed front-end electronics that meet the stringent requirements of the CUORICINO bolometric detector. The principal sections of this front-end are an extra low-noise differential preamplifier, a second stage amplifier with programmable gain, a programmable system for setting the thermistor bias, and a programmable system for setting or nulling the input offset voltage. The remote control capabilities minimizes the need for disruptive physical activity near the detector during data acquisition. We have fabricated the 60 channels that the experiment requires. Two standard 19 in card cages are sufficient to accommodate all of these channels.

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